INSTRUCTION MANUAL

model 153

STROBING VOLTMETER

E-H RESEARCH LABORATORIES, INC.

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INSTRUCTION MANUAL

model 153

STROBING VOLTMETER

October 1971

Serial No. _____

E-H RESEARCH LABORATORIES, INC.

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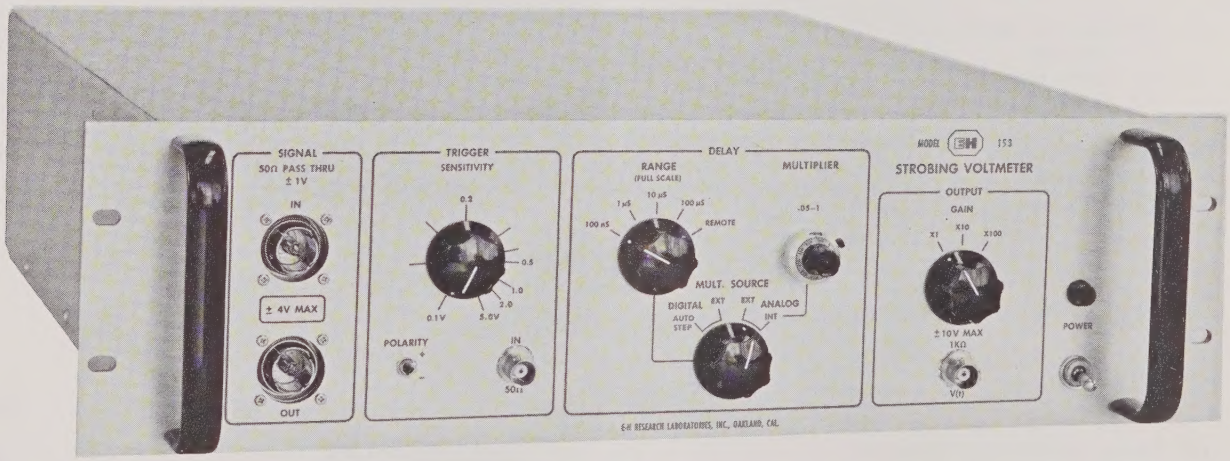

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Figure 1-1 Model 153 Strobing Voltmeter

SECTION 1
SPECIFICATIONS

1-1 GENERAL

The E-H Model 153 is a versatile one-shot sample-and-hold strobing voltmeter capable of making instantaneous voltage amplitude measurements on fast waveforms. The voltage-measurement point-in-time may be delayed from 5 ns to 105 μs following a measurement enabling trigger. Performance parameters may be determined by front-panel mounted controls, or programmed by externally applied logic and analogs.

1-2 SPECIFICATIONS

a. Signal Channel.(Without the use of the ~40 ns internal delay line)

(1) Risetime.<3 ns, equivalent to more than 100 MHz bandwidth.

(2) Noise <0.5 mV pk-pk, referred to the input, (pk-pk noise includes 95% distribution).

(3) Dynamic Range. ±1 V combined dc and peak ac (referred to the dc offset voltage) ±4 V max safe level.

(4) Voltage Accuracy. 1% + noise. In most cases, careful technique can yield voltage amplitude measurements approaching 0.1%.

(5) Signal Input/Output. 50-ohm feedthrough signal path makes the input signal available at the SIGNAL OUT connector for use by other instrumentation, return to the device-under-test, or termination.

(6) Signal Delay Line. 40 ns delay in series with the SIGNAL IN connector permits a measurement effectively coincident with the trigger.

(7) DC Offset. ±1 V externally applied analog into 100 ohm input impedance. Signal is measured relative to the dc offset.

b. Output.

(1) Output Level. ±10 V max, 1 kilohm source impedance.

(2) Voltage Gain. Selectable: X1, X10, or X100. The input signal voltage at strobe time is measured relative to the dc offset voltage. The difference is amplified X1, X10, or X100 and is present at the output connector when the data record trigger occurs.

(3) Holding Time. 250 ms time-constant.

c. Measurement Delay.

(1) Delay Ranges. 100 ns, 1 μs, 10 μs, and 100 μs full scale. Selectable by front-panel switch or external program lines (+3 V keys).

(2) Delay Vernier. Panel-mounted switch selects:

(2a) Front-panel mounted, 10-turn calibrated control. Useable delay from 5% to 105% of selected delay range.

(2b) External, 0 to +5 V delay analog produces 0 to 100% of selected delay range. Input impedance is 1 kilohm.

(2c) D/A Converter, converts 3-decade, 12-line BCD logic to 0 to +5 V delay analog. D/A converter accepts inputs from externally applied BCD logic, (153-1 and -2 options).

(2d) Auto Step. Wherein an internal counter (incremented after each sample) programs the D/A converter The delay interval advances 1/1000th of the selected delay range per measurement, allowing coherent sampling (153-2 option).

(3) Slaving. The delay analog output of the Model 153 may be used to slave the delay analog input of another Model 153. The output of the second Model 153 may be used to drive a third Model 153, etc. Additional slaving configurations are available as optional extras. Contact your E-H Representative, or the factory, for specific information

(4) Delay Accuracy.

(4a) 100 ns range; 0.35% of full scale +1% of the programmed delay.

(4b) 1, 10, and 100 μs ranges; 0.35% of full scale +2% of the programmed delay. Any single range may be calibrated to the accuracy stated for the 100 ns range. BCD programming adds 3% of the programmed delay to the specifications. Accuracy specifications are qualified as follows: (a) valid between 10% and 100% of full scale delay range, (b) a fixed offset error exists between the trigger T zero and the delay range T zero up to 5 ns + 3% of full scale maximum.

(5) Delay Jitter. 0.05% of full scale delay range

d. Trigger Requirements.

(1) Trigger Sensitivity. 100 mV, polarity selectable by panel-mounted switch. Trigger attenuator continuously variable to 50:1. Maximum trigger signal; 20 V attenuated, 4 V unattenuated.

(2) Trigger Holdoff. Measurement cycles will be initiated up to 1 per ms from trigger repetition rates up to 20 MHz. (1 per 10μs optional)

e. Programming.

(1) Delay Ranges. 3 key lines, +3 V on the respective key line will select the 1 μs, 10 μs, or the 100 μs delay range. If none of the keying lines are energized, the delay range is 100 ns. Input impedance for each line is 3 kilohm.

(2) Vernier Delay Analog. 0 to +5 V into 1 kilohm input impedance produces delay from 0 to 100% of the selected delay range.

(3) Vernier Delay Digital (with D/A card installed). Three decade BCD, 12 key lines. +3 V into 5 kilohm impedance per line.

f. Other Outputs.

(1) Delay Analog. 0 to +10 V proportional to vernier delay programmed. 1 kilohm source impedance.

(2) Data Record Trigger. Not less than 1.2 μs trigger pulse occurring approximately 2.5 μs after strobe time. Positive going from ground to +15 V through 1.5 kilohm.

(3) Strobe Time Trigger. 200 ns trigger > 1.0 V positive into 50-ohm coincident with the strobe time.

g. Power Requirements. 105/125 Vac, 50/60 Hz, 100 volt-amps (234 Vac operation available by changing transformer taps).

h. Dimensions. 5-1/4 x 19" panel, 18-3/4" deep (133 x 483 x 476 cm).

i. Weight. 25 lbs. (11.4 kg) net. Domestic shipping package, 35 lbs. (15.9 kg). Export shipping package, 50 lbs. (20.9 kg).

j. Accessories included. 50-ohm termination, GR No. 874 W505; Programming connector, Amphenol No. 5730240.

SECTION 2
OPERATING INFORMATION

2-1 GENERAL

The Model 153 Strobing Voltmeter uses a balanced diode-bridge to isolate its measuring circuitry from its 50-ohm feed-through signal line. The bridge is gated on during a 4 ns strobe period. The time location of the strobe is variable relative to the measurement enabling trigger by panel-mounted controls or by remote program inputs.

The voltage present on the signal line at the end of the strobe period is compared to a dc offset level, and the difference is passed through a memory amplifier chain. The memory amplifier chain has a voltage gain of 10, and a memory time-constant of 250 ms. An additional output amplifier with a voltage gain of 10, and a 10X attenuator allow panel-selectable scale factors of X1, X10, and X100.

The measurement cycle time of the Model 153 is initiated by an externally applied trigger. Once the measurement cycle is initiated, the trigger recognition circuit is locked out for 1 ms. The Model 153 is a single-shot device which is capable of making 1000 measurements per second. The fixed trigger lockout period allows time for auxiliary equipment to accept the measurement information supplied by the Model 153 (data rates to 100 kHz are optional).

2-2 FUNCTION OF FRONT PANEL CONTROLS AND CONNECTORS

a. SIGNAL IN and SIGNAL OUT Connectors. A 50-ohm loop-through signal line for the input signal to be measured. There is 40 ns of delay between the SIGNAL IN connector and the measurement bridge.

b. TRIGGER SENSITIVITY. Controls an attenuator between the TRIGGER IN connector and the trigger discriminator. Permits triggering on signals from 100 mV to 20 V.

c. TRIGGER POLARITY Switch. Controls the input connections to the trigger discriminator. Permits triggering on either positive or negative trigger signals.

d. TRIGGER IN Connector. A 50-ohm input for the measurement-enabling trigger signal.

e. DELAY RANGE Switch. A 5-position switch which selects either the 100 ns, 1 μs, 10 μs, 100 μs delay range, or selects remote programming for the delay range.

f. DELAY MULT. SOURCE Switch. Selects the source of the dc analog voltage to be used as the vernier delay multiplier. In the DIGITAL/AUTO STEP position, the internal counter programs the D/A converter which in turn is used as the vernier delay multiplier. In the DIGITAL/EXT. position, the counter is held in its reset condition so that external signals can program the D/A converter to set the delay vernier. In the ANALOG/EXT. position, the dc voltage applied to the rear-mounted DELAY ANALOG IN connector is used to set the delay vernier. In the ANALOG/INT. position the panel-mounted MULTIPLIER control determines the vernier delay multiplier.

g. DELAY MULTIPLIER. A 10-turn control which determines the vernier delay multiplier when the MULT. SOURCE switch is in the ANALOG/INT position. The control is continuously adjustable from 5% to 105% of the selected delay range.

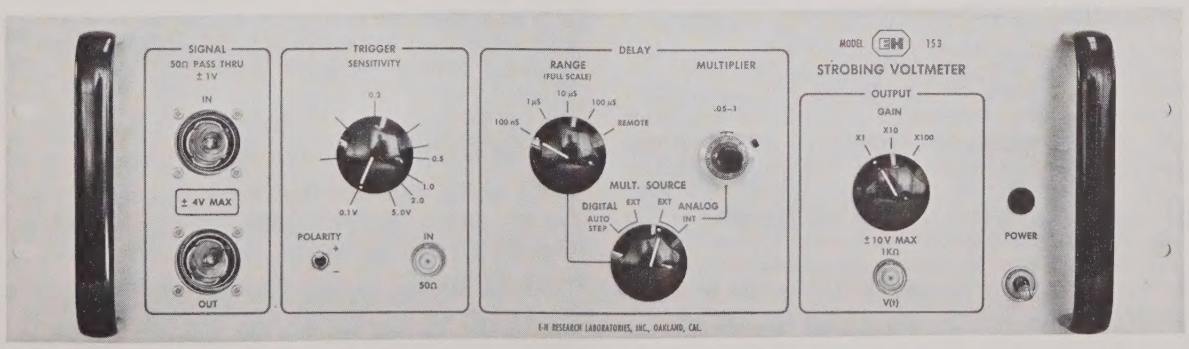

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Figure 2-1 Model 153 Front Panel

h. **OUTPUT GAIN Switch.** Selects the overall voltage gain of the Model 153. The output voltage may be 1, 10, or 100 times the input voltage at strobe time, with the limitation that the output voltage is not more than ±10 V.

i. **V(t) Connector.** The measurement output connector. The voltage present at this connector is proportional to the difference between the input signal and the dc offset voltage at strobe time. Source impedance is 1 kilohm, and the decay time-constant is 250 ms.

j. **POWER Switch.** Applies or disconnects the primary power to all circuits in the Model 153. The associated pilot light indicates power on.

2-3 FUNCTION OF REAR PANEL CONNECTORS

a. **J301.** Primary power-line input, either 117 Vac or 234 Vac, 50/60 Hz, depending on the connections to the primary of the power transformer. See the power supply schematic for the 117/234 volt option.

b. **J307.** Remote programming connector. Provides connections to remote programming leads.

c. **STROBE TIME TRIGGER OUTPUT CONNECTOR.** Provides a 200 ns trigger whose leading edge is coincident with the sampling gate.

d. **DATA RECORD TRIGGER OUTPUT CONNECTOR.** Provides a 1.2 μs trigger occurring approximately 2.5 μs after strobe time. The presence of a trigger at this connector indicates that the measurement has been made, and an output is ready for use at the front panel-connector, V(t).

e. **DELAY ANALOG OUT Connector.** Provides an output voltage between 0 and +10 V proportional to the vernier delay multiplier analog regardless of the source of the analog. Source impedance is 1 kilohm.

f. **DELAY ANALOG IN Connector.** Input connector for externally applied vernier delay multiplier analog. When the front panel DELAY MULT. SOURCE switch is in the ANALOG/EXT position, the voltage at this input connector determines the vernier delay multiplier factor. Input impedance is 1 kilohm, sensitivity is +5 V for full scale delay on the selected delay range.

g. **OFFSET IN.** 100-ohm connector.

2-4 OPERATION

a. **Waveforms.** The waveforms which fall within the measurement capability of the Model 153 can contain appreciable frequency components in excess of 100 MHz. If any of these high-frequency components are attenuated through the use of connectors, cables, or attenuators that do not have a flat frequency response beyond 100 MHz, degradation of the waveforms will result. Mismatch effects can also degrade pulse waveforms; therefore, consideration and care must be taken to preserve the quality of signal and trigger waveforms when coupling to the system or to the device-under-test.

If the signal source-impedance of the device or system under test is other than 50-ohm, use an impedance matching device so that mismatch effects will not degrade the waveform to be measured. Return the signal loop-through output connector to an effective 50-ohm pure-resistive load. The signal loop-through output connector may be either terminated in 50 ohms at the panel connector, or returned to a 50-ohm environment.

Make sure that all connectors, attenuators and cables are of proper impedance and have a flat frequency response in excess of 100 MHz. Use high-quality 50-ohm coaxial cable, such as RG213/U. For best results, use short cables, since long cables tend to attenuate the high frequency components of fast waveforms. General Radio (GR) 874 series coaxial connectors are recommended for the signal path into and out of the Model 153.

b. **Triggering.** The measurement cycle of the Model 153 must be initiated by an externally applied trigger. The triggering signal initiates a 1 ms hold-off interval during which the trigger recognititon circuit is locked out. Triggering signals may be applied with repetition rates up to 20 MHz. Triggering signals which occur during the 1 ms hold-off interval are not recognized. The trigger recognititon circuit will accept the next trigger which agrees with the trigger polarity selector switch and the sensitivity control after the hold-off interval terminates.

Provisions are made in the trigger recognition circuit to prevent multiple triggering from a single wide triggering signal. The trigger signal must be at zero volts at the end of the hold-off interval, or revert to zero after the hold-off interval before a new cycle can be initiated.

The trigger input connector is internally terminated in 50 ohms. The triggering signal should be from a 50-ohm source, or impedance matched to the 50-ohm trigger input. It should have a fast rise time, in the order of 1 ns, to avoid the uncertainty of where triggering occurs on the rise of the triggering waveform. The triggering signal should also have a finite jitter-free time relationship to the signal to be measured. These considerations are particularly important when making measurements on the 100 ns delay range.

The Model 153 has an effective delay offset (T zero) for each delay range. The effective T zero will be within 5 ns ±3% of the selected delay range from the time triggering occurs. Programmed delays are relative to this effective T zero. As long as the calibration of the instrument is not disturbed, the effective T zero for each individual range can be expected to remain fixed relative to the trigger.

c. **Signal Handling.** For reliable measurements the input signal to the Model 153 must be handled in accordance with good fast-pulse techniques. All cabling, connectors and attenuators must be capable of transporting the signal to be measured through the signal loop-through path and to an effective 50-ohm termination. The Model 153 will measure the voltage present at its sampling bridge at the end of the measurement strobe.

If the applied signal has been degraded or if reflections are present, due to improper signal handling techniques, the measurement will be erroneous and misleading.

The signal handling portion of the Model 153 is confined to a 50-ohm coaxial feedthrough loop which includes 27 ft. of RG214. This 40 ns of delay in the signal path allows time for switching in the trigger recognition and delay circuits. On the 100 ns delay range, with minimum delay programmed, it is possible to strobe in advance of a fast-rise signal which is time

coincident with the trigger. When the Model 153 is used as a coherent sampler, this permits display of a leading edge which is coincident with the trigger.

For maximum bandpass capability, the delay cable may be removed. In this case, the effective delay interval will be 40 ns longer than the same programming would produce with the delay cable.

d. Delay Interval. The input signal voltage amplitude is sampled after a predetermined delay interval. The delay interval is initiated by the trigger and is continuously adjustable from 5 ns to 105 μs in four delay ranges. The delay interval may be determined by front-panel controls or by external programming.

To determine the delay interval, one of the four delay ranges must be selected and a dc analog must be provided. Full scale on the four ranges are: 100 ns, 1 μs, 10μs and 100 μs. The dc delay analog in is a voltage from 0 to +5 V corresponding to 0 to full scale on the selected delay range.

The desired delay range may be selected by the front-panel DELAY RANGE switch, or if the switch is in the REMOTE position, the delay range may be selected by applying +3 V to the appropriate keying line in the rear-mounted programming connector, J302. There are three delay range keying lines, one each for the 100 μs, the 10 μs, and the 1 μs delay ranges. If none of these ranges are selected, the delay range is 100 ns full scale.

The selection of the source for the vernier delay analog voltage is independent of the selection of the delay range. The panel-mounted DELAY MULT. SOURCE switch selects DIGITAL/AUTO STEP, DIGITAL/EXT., ANALOG/EXT. or ANALOG/INT.

(1) When ANALOG/INT. is selected, the panel-mounted DELAY MULTIPLIER potentiometer selects the vernier delay voltage. The DELAY MULTIPLIER is continuously adjustable from 5% to 105% of the selected delay range.

(2) When ANALOG/EXT is selected, the voltage at the rear-mounted DELAY ANALOG IN connector provides the vernier delay analog voltage. The input impedance is 1 kilohm. The sensitivity at the DELAY ANALOG IN connector is +5 V for full scale delay on the selected delay range.

The output from the DELAY ANALOG OUT connector is 0 to +10 V from a 1 kilohm source impedance. When the DELAY ANALOG OUT from one Model 153 is connected to the DELAY ANALOG IN on another Model 153, the 1 kilohm source impedance and the 1 kilohm input impedance makes a 2:1 voltage divider. Thus the full scale output voltage matches the full scale input voltage, and one Model 153 can provide the DELAY ANALOG IN for another Model 153. The second Model 153 will be programmed for the same delay interval if both Model 153s have the same delay range selected.

The buffer amplifier in the Model 153 requires about 100 μs to slew to a new delay analog voltage. At least 100 μs should be allowed between the application of a new delay analog input and triggering of the measurement cycle.

(3) When DIGITAL/EXT. is selected, the output of the D/A converter card provides the vernier delay analog voltage. The D/A card permits digital programming of the delay analog voltage from an external source. In this mode of operation, the delay vernier is determined by the BCD logic on the 12 external programming lines. Each of the 12 key lines has 5 kilohm impedance. Logic 1 is +3 V and logic 0 is 0 V. The 12 key lines accept 3 decades of logic in a 1-2-4-8 BCD code. The least significant bit represents 0.1% of the selected delay range.

(4) In the DIGITAL/AUTO STEP mode, the D/A card accepts inputs from the internal BCD counter (if the counter card is installed). In this mode of operation, the count held by the counter is increased by one bit each time a measurement is made, permitting coherent sampling with 1000 dots/display density.

e. Output Data. The data output from the Model 153 is available at the front panel BNC connector labeled V(t). The output is a voltage waveform from a 1 kilohm source impedance. The output voltage rises to its peak value within 4 μs after strobe time and then decays with a 250 ms time-constant. The peak output voltage is between +10 and -10 V, and is proportional to the difference between the input signal voltage amplitude and the dc offset voltage at strobe time. It is either 1, 10 or 100 times the measured input voltage, depending on the position of the OUTPUT GAIN control on the front panel.

f. Coherent Sampling. With the digital counter card and the D/A converter card installed, the Model 153 may be used as a coherent sampler.

The digital counter card is a 3-decade BCD counter which increases the count by 1 bit after each measurement strobe. The output of the digital counter is BCD logic on 12 keying lines, which are connected to the D/A converter card and the rear-mounted programming connector, J302. Since the counter has three decade capacity, it delineates 1000 input bits.

The D/A card is a 3-decade digital-to-analog converter. The inputs to the D/A card are the 12 logic lines from the digital counter and/or the rear-mounted programming connector, J302. The D/A card converts the BCD logic on the 12 keying lines to an analog between 0 and +5 V to be used as the vernier delay analog. Thus the selected delay range is divided into 1000 discrete steps, one of which is selected by the logic present on the BCD keying lines.

If the D/A card is driven from the counter card, the delay interval is increased by 1/1000 of the full scale delay range after each measurement strobe. Thus, 1000 successive triggers will scan from 0 to delay to full scale of the selected delay range.

The waveform at the DELAY ANALOG OUT connector would be a 1000 increment stair step from 0 to +10 V. The waveform at the V(t) output would be the voltage amplitude points on the input signal waveform that corresponds to each of the 1000 delay intervals.

The DELAY ANALOG OUT waveform can be used as the horizontal deflection voltage, and the V(t) output can be used as the vertical deflection voltage to produce a coherent sampling display on a relatively unsophisticated display device.

g. External Programming. The two functions that may be externally programmed are the delay range and the delay vernier. If the D/A converter board is installed, the delay vernier may be programmed either with 3-decade BCD logic or with a 0 to +5 v analog.

The delay range is programmed by applying +3 V to one of three delay range keying lines. There is one keying line each for the 1 μs, 10 μs, and 100 μs delay ranges. If all three of these keying lines are at 0 V the 100 ns delay range is selected. The delay ranges are not mutually exclusive. Care must be taken not to program two or more ranges at the same time. For example, if +3 V is applied simultaneously to the 100 μs and the 10 μs keying line, the effective delay range will be approximately 110 μs. The resulting measurement will probably be misleading. Refer to the change page section of this manual for pin connections on the programming connector, J307.

The delay vernier may be externally programmed by applying a dc analog between 0 and +5 V to the DELAY ANALOG IN connector, mounted on the rear plate. 0 V corresponds to 0 delay, and +5 V corresponds to full scale delay on the selected delay range. The voltage applied to the DELAY ANALOG IN connector may select delays from 0 to 105% of the selected delay range. Normally the programming should not select less than 10% of the selected delay range. If a delay of less than 10% of full scale is desired, the next faster range should be used.

If the D/A converter board is installed, the delay vernier may be externally programmed by applying-3-decade BCD logic to the 12 BCD keying lines. The D/A converter board as normally supplied is no-latching, and accepts 3 decades of 1-2-4-8 BCD logic. Additional components may be added to the D/A converter board, or component values changed to accommodate a wide variety of logic. Consult your E-H Representative, or the factory, for specific information.

In the DIGITAL/EXT. mode, the counter card (if installed) is held in its reset position to prevent its interfering with the external D/A data to the D/A converter. In the DIGITAL/AUTO STEP mode, the external D/A must be inhibited to allow the counter to properly program the D/A converter.

SECTION 3
THEORY OF OPERATION

3-1 GENERAL

This section of the manual contains an electrical description of each circuit in the Model 153 Strobing Voltmeter. A block diagram is included in the drawings section showing the overall relationship of the various circuits. Schematic circuit numbers are used to identify components in the circuit descriptions. Refer to the specific schematics in the drawings section to supplement the following discussion.

The Model 153 Strobing Voltmeter samples the instantaneous voltage amplitude of the signal applied to its 50-ohm loop-through input. The time of sampling is delayed a predetermined interval after an externally-applied trigger. The delay interval may be set by front-panel controls, by externally applied programming, or the delay interval may be sequentially stepped by an internal counter.

3-2 BLOCK DIAGRAM

a. Measurement-enabling Trigger. The measurement-enabling trigger is applied to a panel-mounted BNC connector. The input impedance is 50 ohms. A panel-mounted sensitivity control permits adjusting the trigger sensitivity from 100 mV to 20 V. A panel-mounted polarity-selector switch permits triggering on a positive trigger signal or a negative trigger signal.

b. Trigger Discriminator. The trigger discriminator amplifies the trigger signal and drives the trigger shaper.

c. Trigger Shaper. The trigger shaper is a tunnel diode and a power amplifier. Providing the hold-off clamp has released from the previous measurement cycle, the trigger shaper switches the bistable multi.

d. Bistable Multi. The bistable multi is a fast-switching bistable multivibrator. It turns on the ramp gate, and is switched for the first 500 μsec of the 1000 μsec hold-off interval.

e. Ramp Gate. The ramp gate is a current commutating pair. In its quiescent condition it provides current to the hold-off switch. During the 500 μsec following triggering, when the bistable multi is switched, the ramp gate turns off the current normally supplied to the hold-off switch, and gates on the ramp generator.

f. Hold-off Switch. The hold-off switch establishes the 1000 μsec hold-off interval. The hold-off interval is divided into two intervals of approximately 500 μsec each. All of the logic functions are performed during the first 500 μsec interval. The second 500 μsec interval permits the circuitry to return to its quiescent condition before being re-triggered. The hold-off switch resets the bistable multi after the first 500 μsec of the hold-off interval. An output from the hold-off switch drives the hold-off clamp for the full 1 ms hold-off interval.

g. Hold-off Clamp. The hold-off clamp effectively shorts out the trigger shaper for the 1 ms hold-off interval. The applied trigger signal must revert to near zero after the hold-off interval has elapsed before the hold-off clamp will release the trigger shaper. Thus a trigger signal of more than 1 ms width can not initiate more than one measurement cycle.

h. Ramp Generator. The ramp generator, when gated on by the ramp gate, produces a linear delay ramp. The time duration of the delay ramp is determined by the ramp range selector. The output of the ramp generator provides an input to the ramp comparator, and also provides an input to the counter driver.

i. Ramp Range Selector. The ramp range selector determines the time duration (slope) of the delay ramp. The ramp range selector can be operated by a front-panel mounted control, or by external programming. If external programming is used, +3 V on the proper keying line will select the 1 μs, 10 μs, or 100 μs range. If none of these three ranges are selected, the delay ramp will be 100 ns.

j. Delay Analog Buffer. The delay analog buffer accepts the 0 to 5 V delay analog voltage. It provides an isolated output to the ramp comparator and to the DELAY ANALOG OUT jack. The delay analog buffer is a feedback stabilized amplifier with a voltage gain of 2 and an output impedance of 1 kilohm.

The input to the delay analog buffer is selectable by a front-panel control. The input can be from the panel-mounted 10 turn control, from the rear-mounted DELAY ANALOG IN jack, or from the internal D/A converter.

The 2X gain incorporated in the delay analog buffer permits driving a 1 kilohm source impedance and achieving the same dc level across the load as at the input of the buffer amplifier. The alternative would be an amplifier with a gain of 1 and near zero output impedance. Such a low output impedance amplifier would not provide short circuit protection.

The delay analog output of the Model 153 will provide the delay analog input for another Model 153 directly, since the gain of 2 and the 1 kilohm output impedance is compatible with the 1 kilohm input impedance.

k. Ramp Comparator. The ramp comparator is a voltage-amplitude discriminator pair. The two inputs are the

range ramp from the ramp generator, and a dc voltage level from the delay analog buffer. When the range ramp reaches amplitude-coincidence with the delay analog voltage, the ramp comparator triggers the delayed pulse generator.

l. Delayed Pulse Generator. The delayed pulse generator is a one-shot multi-vibrator. It generates a 200 ns wide delayed pulse. The leading edge of the delayed pulse follows the measurement-enabling trigger by a time interval equal to the programmed delay. The leading edge of the delayed pulse triggers the strobe generator and the trailing edge triggers the memory gate generator and the data record trigger delay.

m. Counter Driver. The counter driver clamps the delay ramp at about 110% of full scale. After the full scale range interval has elapsed, the counter driver produces an output bit to increase the BCD counter by 1.

n. BCD Counter. The BCD counter is a 3-decade counter. One bit is added from the counter driver after each range ramp is completed. The output of the BCD counter drives the D/A converter and/or the 12 external BCD logic lines.

o. D/A Converter. The D/A converter is a digital-to-analog converter. It is either driven by the internal BCD counter or from external BCD programming. When the D/A converter is driven by the BCD counter, the output is a 1000 increment voltage stair-step from 0 to +5 V. When the D/A converter is driven from the external programming lines, the output is an analog equivalent of the numerical value of the BCD logic. In either case, the output of the D/A converter is available as the delay analog voltage. It determines the vernier delay when the panel-mounted DELAY MULT. SOURCE switch is in either DIGITAL position.

p. Strobe Generator. The strobe generator is triggered by the leading edge of the delayed pulse. The output of the strobe generator is a 4 ns strobe at the end of the delay interval. During the strobe pulse, the applied signal is connected through the sampling bridge to the first memory input.

q. DC Offset Amplifier. The DC offset amplifier isolates the dc offset voltage source and biases the first memory amplifier. The signal to be measured is sampled relative to the dc offset voltage. The output of the Model 153 is proportional to the difference between the applied signal and the dc offset voltage.

r. First Memory Amplifier. The first memory amplifier amplifies the signal sample by a factor of 4, and drives the second memory amplifier through the memory gate bridge.

s. Memory Gate Generator. The memory gate generator is triggered at the trailing edge of the delayed pulse by the strobe time trigger generator. The output is a 1.2 μsec pulse starting 200 ns after strobe time which gates on the memory gate.

t. Strobe Time Trigger Generator. The strobe time trigger generator buffers and amplifies the 200 ns pulse from the memory gate generator which goes to the STROBE TIME TRIGGER connector on the rear panel. Its trailing edge triggers the memory gate generator and the data record trigger delay.

u. Memory Gate Bridge. The memory gate bridge connects the output of the first memory amplifier to the input of the second memory amplifier for the duration of the 1.2 μsec memory gate.

v. Memory Gate Amplifier. The second memory amplifier further amplifies the signal sample by a factor of 2.5. The second memory has a long-decay time-constant, approximately 250 ms. Gain adjustments and dc level adjustments are made in the second memory amplifier. The voltage gain from the signal input to the output of the second memory amplifier is 10X.

w. Voltage Gain Control. The voltage gain of the output amplifier is selectable by a front-panel control. The output of the second memory amplifier may be attenuated by a factor of 10, connected directly to the output jack, or amplified by a factor of 10. This allows an over-all voltage gain from the input of 1, 10 or 100. The output amplifier provides the output signal to the panel-mounted output jack V(t).

x. Data Record Trigger/Delay. The delay is triggered at the trailing edge. The output of the 2.5 μsec delay drives the data record trigger generator. The delay allows the output at V(t) to rise to its peak amplitude before informing associated equipment that the output data is ready for use.

y. Data Record Trigger Generator. The data record trigger generator output signals associated equipment that the output from the Model 153 is present at the output jack, V(t), and ready to be used. The data record trigger is a 1.2 μsec wide pulse that starts 2.5 μsec after strobe time.

3-3 CIRCUIT DESCRIPTION

a. Measurement Interval. The measurement interval is initiated by a trigger applied to the 50-ohm panel-mounted TRIGGER IN jack. The trigger signal may be of either polarity as selected by the panel-mounted TRIGGER POLARITY switch. The trigger sensitivity adjustment permits triggering from signals of 100 mV to 20 V in amplitude. The triggering signal is applied to the discriminator through the balun transformer, T201. The purpose of T201 is to provide push-pull drive from the single-ended input. Triggering is accomplished by a negative-going waveform at pin 1 of the printed circuit board.

b. Trigger Discriminator. The trigger discriminator is a push-pull amplifier pair made up of Q1 and Q2. R23 and R65 from the -15 V supply provides a constant 10 mA of emitter current to be shared by Q1 and Q2. In the quiescent condition with no trigger signal applied, Q1 conducts a little more than 5 mA, and Q2 conducts a little less than 5 mA, determined by the difference in their individual emitter resistor, R22 and R24. Q1 and Q2 each have a tunnel diode in their collector circuit which will snap to its high voltage state when driven with 10 mA or or more. When a trigger signal is applied which agrees with the trigger polarity selector switch and sensitivity setting, Q2 increases conduction beyond 5 mA, and Q1 reduces conduction below 5 mA.

c. Trigger Shaper. The trigger shaper is made up of the tunnel diode, CR4, and the voltage-amplitude discriminator pair, Q4 and Q5. In the quiescent condition, with no trigger applied, the tunnel diode CR4 is in its low voltage state (100 mV), Q4 is not conducting and Q5 conducts all of the

common emitter current through R5 from the +15 V supply. The divider made up of R7 and R8 establishes the base voltage of Q5 at 250 mV below the +5 V supply. The two voltage states of CR4 are 100 mV and 500 mV. Q4 does not conduct when CR4 is in its low voltage state. Q4 conducts all of the common emitter current through R5 when CR4 is in its high voltage state.

Triggering is accomplished when CR4 snaps from its low voltage state to its high voltage state. The current threshold for CR4 is 10 mA. A constant 5 mA is furnished to CR4 through R26 from ground. The remainder of the current for CR4 is collector current from Q2 which is normally less than 5 mA. When a negative-going trigger signal is applied to the base of Q1, the collector current in Q2 increases and pushes CR4 over its current threshold into its high voltage state and causes current to switch from Q5 to Q4.

During the 1 ms hold-off interval following trigger, Q3 conducts at saturation and effectively bypasses CR4. During this hold-off interval, even if trigger signals are applied to the trigger discriminator pair, collector current for Q2 is conducted through Q3 and the tunnel diode CR4 remains in its low voltage state. Triggering cannot occur again until the hold-off clamp, Q3, is turned off, making current available to CR4.

d. Bistable Multi. The bistable multi, made up of Q6 and Q7, is switched by the collector current from Q4. The bistable multi remains switched for the first half of the hold-off interval. The quiescent condition before triggering is with Q6 conducting and Q7 not conducting. Collector current from the trigger shaper, Q4, pulls the base of Q6 in a positive direction, turning off Q6 and turning on Q7.

e. Ramp Gate. The ramp gate is a current switching output stage for the bistable multi. When the bistable multi is in its quiescent condition, prior to triggering, Q9 conducts all of the common emitter current through R32 from the -15 V supply. Q10 does not conduct in the quiescent condition. When the bistable multi switches as a result of triggering, Q9 turns off and Q10 conducts all of the common emitter current. There are two outputs from the ramp gate. Prior to triggering, Q9 provides current to the hold-off switch. During the first 500 μs of the hold-off interval when the bistable multi is switched, Q9 turns off the current to the hold-off switch. Prior to triggering, when Q10 is not conducting, R35 provides base current for the ramp generator. When triggering occurs and Q10 conducts, the collector of Q10 is pulled down to one junction drop below ground, defined by the clamp diode CR10. During the first 500 μs of the hold-off interval, R35 does not provide base current to the ramp generator.

f. Hold-off Switch. The hold-off switch is made up of Q11, Q12 and Q13. The timing capacitors, C3 and C18, define the hold-off interval. Q12 and Q13 are a current switching pair. They share a common emitter current through R10 from the +25 V supply. The base voltage of Q13 is defined by the +15 V supply. The base voltage for Q12 is above or below the 15 V supply, depending on whether or not Q11 conducts. In the quiescent condition before triggering, Q11 conducts the current supplied from the ramp gate, Q9. The base of Q11 is referenced to the +5 V supply through R9, and Q11 acts as an emitter follower to hold the voltage on C3 and C18 to 1 junction drop below the +5 V supply. Collector current from Q11 holds the base of Q12 below the +15 V supply and Q12 conducts all of the current supplied through R10 from the +25 V supply. In the quiescent condition, Q13 does not conduct.

When triggering occurs; the current supplied by Q9 is turned off, Q11 stops conducting, the base of Q12 goes more positive than the +15 V supply, and Q13 conducts all of the current through R10 from the +25 V supply. C3 and C18 charge toward the +25 V supply through R14 and R13.

The time constant defined by C3, C18, R14 and R13 determines the first half of the hold-off interval. When C3 and C18 charge to a voltage positive enough to cause Q8 to conduct, the bistable multi is switched back to its quiescent condition and Q9 again supplies current. The time constant defined by C3, C18 and collector current from Q9 determines the second half of the hold-off interval. Collector current from Q9 discharges C3 and C18 back down to their quiescent voltage of less than 5 V. The discharge current provided to C3 and C18 is approximately equal to the charge current provided through R13. The charging time of C3 and C18 defines the first half of the hold-off interval, and the discharge time defines the second half. When C3 and C18 have discharged below +5 V, Q11 goes back into conduction providing base current to Q12. Q12 conducts the common emitter current from R10, and Q13 is turned off. The hold-off interval is made up of two 500 μs intervals. The first interval is with the bistable multi switched, Q9 turned off, and C3 and C18 charging in a positive direction. The second 500 μs interval is with the bistable multi switched back to its quiescent condition and Q9 discharging C3 and C18. The hold-off interval is not terminated until C4 and C18 are discharged below 5 V and Q11 goes back into conduction.

g. Hold-off Clamp. The hold-off clamp, made up of CR1 and Q3, effectively bypasses the tunnel diode CR4 during the hold-off interval. The quiescent condition of the hold-off clamp before triggering is with CR1 in its high voltage state and Q3 not conducting. In this condition, collector current from Q2 in the trigger discriminator circuit plus the current from R26 is available to drive CR4. During the hold-off interval when Q13 is conducting, collector current from Q13 holds CR1 in its low voltage state and causes Q3 to conduct at saturation. When the hold-off interval is over and Q13 is turned off, CR1 will snap back to its high voltage state, providing Q1 in the trigger discriminator circuit is conducting its quiescent collector current. If the initial trigger signal is still present on the trigger discriminator when hold-off is terminated, Q2 is still conducting more than its quiescent 5 mA, Q1 is conducting less than its quiescent 5 mA, and CR1 will not snap back to its high voltage state. The trigger signal on the trigger discriminator must revert to near zero after the hold-off interval for Q1 to conduct its quiescent current before CR1 will snap back to its high voltage state and turn off Q3. This provision is incorporated to prevent a wide trigger signal from initiating more than one measurement cycle. If the trigger discriminator is in its quiescent condition when the hold-off interval is over, collector current from Q1 plus the current from R3 is sufficient to snap CR1 back to its high voltage state and turn off Q3. Current from Q2 is then available to CR4 to initiate a new trigger.

h. Ramp Generator. The ramp generator includes Q14, Q15 and the charging capacitor, C6, C10, C11 and C12. Q15 is a constant current source of about 20 mA from the +15 V supply. Before triggering, Q14 conducts at saturation, holding its collector near ground, because of the base current supplied to it by R35 in the ramp gate circuit. When triggering occurs, Q10, in the ramp gate circuit, conducts

pulling the base of Q14 one junction drop below ground. Q14 is turned off for the first half of the hold-off interval (500 μs following trigger) and the constant current provided by Q15 charges C6. The waveform provided to the ramp comparator by C6 is a linear positive-going ramp. The ramp starts near ground and runs up to +5 V in the time determined by the ramp range selector. The ramp continues to charge past the end of the range to about +6 V where it is clamped by the counter driver. The ramp stays at the +6 V level until the ramp gate switches back to its quiescent condition, when Q14 again conducts at saturation and discharges the ramp range capacitors back to near ground.

i. Ramp Range Selector. The ramp range selector is made up of Q16, Q17, Q18 and the charging capacitors C6, C10, C11 and C12. The inputs to the ramp range selector are from the front panel range selector switch or from external programming logic through the buffer amplifiers on the buffer board. When base current is provided to Q16, Q17 or Q18, the respective charging capacitor, C10, C11 or C12, in their collector circuit, is in parallel with the charging capacitor, C6, modifying the time interval required for the ramp to reach its full scale voltage level of +5 V. The ramp ranges are not mutually exclusive and care must be taken in programming to avoid two simultaneous ranges. The clamp diodes CR20, CR21 and CR22 provide a discharge path for their respective charging capacitors.

j. Delay Analog Buffer. The delay analog buffer is a voltage-feedback stabilized amplifier with a voltage gain of 2. The input of the delay analog buffer is a voltage between 0 and +5 V which determines the portion of the selected delay range to be used. Zero voltage input provides no delay and +5 V provides full scale delay on the selected delay range. The output of the delay analog buffer makes the delay analog voltage available at the DELAY ANALOG OUT jack from a 1 kilohm source impedance. The output of the delay analog buffer also provides the dc reference voltage to the ramp comparator.

The input to the delay analog buffer is selected by the panel-mounted DELAY MULT. SOURCE switch. The delay analog voltage source can be: (1) a panel-mounted 10 turn dial, (2) the DELAY ANALOG IN jack or, (3) the output of the D/A converter. A dc offset adjustment is provided in the output of the delay analog buffer so the dc level to the ramp comparator will agree with the ramp voltage.

The delay analog buffer is made up of Q1, Q2, Q3 and Q4. Q1 and Q2 are connected as a voltage-amplitude discriminator pair which share a common source of emitter current through R8 from the -25 V supply. Q1 and Q2 each conduct about 1 mA. When a + voltage is applied to the base of Q1, the increase in collector current in Q1 provides base current to Q3. The collector current of Q3 pulls the base voltage of Q2 up to equal the base voltage of Q1. The current flow through R11, required to hold the base voltage of Q2 equal to the base of Q1, must also flow through R10. Since R10 and R11 are the same value, the voltage at the collector of Q3 is twice the voltage at the base of Q2. The network R12 and R13 provides for forcing additional current, either + or -, through R10. This permits a small adjustment in output dc level to compensate for the difference in the base-emitter junction drops of Q1 and Q2.

When the delay analog output is used to drive the delay analog input of another Model 153, the 1 kilohm input impedance of the second Model 153, together with R15, make up a 2:1 divider. This divider and the 2X voltage gain provided by the delay analog buffer makes the input voltage to the second Model 153 the same as the delay analog input voltage to the first Model 153.

When the delay analog input has selected the full delay range, +5 V is present at the input of the delay analog buffer. Since the delay analog buffer has a voltage gain of 2, the voltage at the collector of Q3 will be +10 V. The reference voltage provided to the ramp comparator will be +5 V (about 0.5 V of fixed dc offset and 4.5 V of dynamic control voltage). The voltage divider made up of R16 and R17 on the buffer board and R43, R42 and R44 on the trigger board divides the dynamic control voltage output of the delay analog buffer down to 4.5 V as a reference for the ramp comparator. Q4 and its associated components make up a constant current source of about 3 mA. Since the delay ramp starts at +0.5 V, it is necessary to offset the delay analog reference voltage by an equal amount.

k. Range Ramp Comparator. The range ramp comparator is a voltage-amplitude discriminator made up of Q19, Q20, Q21 and Q22. The inputs to the ramp comparator are the delay ramp at the base of Q19 and the delay analog reference voltage at the base of Q20. The voltage amplitude discriminator pair, Q19 and Q20, share a common source of emitter current through R38 from the +25 V supply. Before triggering occurs, the base of Q19 is held clamped at +0.5 V by Q14 in the ramp generator. The base of Q20 is some voltage between +0.5 V and +5 V determined by the delay analog input through the delay analog buffer. Q19 conducts all the emitter current available and Q20 is turned off. Q22 and Q21 are output amplifiers for Q19 and Q20. Q22 and Q21 share a common source of emitter current through R45 from the -15 V supply. When Q19 is conducting, before triggering, Q22 conducts all the current available through R45, and Q21 is turned off.

When triggering occurs, the voltage at the base of Q19 runs up in a positive direction with a slope determined by the ramp range selector. When the voltage at the base of Q19 is equal to the voltage at the base of Q20, Q20 starts to conduct providing base current to Q21. Collector current from Q21 pulls the base of Q20 sharply negative to speed up the current switching from Q19 to Q20. Current switching from Q19 to Q20 occurs at a time interval after triggering determined by the ramp range selected and the dc delay analog programmed. When conduction is transferred from Q19 to Q20, conduction is also transferred from Q22 to Q21. The interruption of current flow through L1 in the collector circuit of Q22 produces a sharp positive spike which triggers the delayed pulse generator.

l. Delayed Pulse Generator. The delayed pulse generator is a one-shot multivibrator which produces a 200 ns pulse starting at the end of the programmed delay interval. The leading edge of the delayed pulse triggers the strobe generator and the trailing edge triggers the memory gate generator and the data record trigger delay.

The delayed pulse generator is made up of the one-shot multivibrator, Q23 and Q24, and the output amplifier pair, Q25 and Q26. The quiescent condition for the delayed pulse generator is with Q23 and Q26 conducting, and with Q24 and Q25 turned off.

The quiescent base voltage for Q23 is established by voltage divider, R47, CR15A, R18A and the clamp diode CR17. The clamp diode CR17 holds the anode of CR15A at one junction drop below ground. This sets the quiescent base

voltage for Q23 at 5.7 V. Collector current from Q23 forward biases the clamp diode CR16 holding the anode of the zener diode CR15B at one junction drop above ground. This sets the quiescent base voltage of Q24 and Q25 at +6.9 V. Q23 conducts all of the current supplied through R49 and R50 from the +15 V supply. Q23 also conducts the current supplied through R51 and CR18 from the +15 V supply.

When the one-shot multivibrator is triggered by a positive pulse from the ramp comparator, Q23 turns off. The collector voltage of Q23 drops below ground, providing drive to the base of Q24. Q24 conducts the current through R51 from the +15 V supply and also the current through R50 and R49 through C9. C9 can support the current through R49 and R50 for 200 ns after which time the emitter of Q23 has gone far enough positive for Q23 to go back into conduction, turning off Q24 and reverting the one-shot multivibrator back to its quiescent condition.

In the quiescent condition, Q26 conducts the current supplied through R53 from the +15 V supply and Q25 is turned off. During the 200 ns delayed pulse, Q25 conducts the current supplied through R53 and Q26 is turned off. This produces a positive-going delayed pulse at the collector of Q25 and a negative-going delayed pulse at the collector of Q26. The leading edge of the output from Q25 triggers the strobe generator. The output from Q26 drives the strobe time trigger generator.

m. Counter Driver. The purpose of the counter driver is to clamp the delayed ramp when it has reached +6 V and to produce an output to increase the digital counter by 1 bit. The counter driver is made up of Q27 and Q28.

The quiescent condition of the counter driver is with both Q27 and Q28 turned off. The base of Q27 is held at +5 V by the divider made up of CR6 and R19. The range ramp drives the emitter of Q27. With Q27 not conducting, the base of Q28 is held at one junction drop below ground by the divider R18 and CR7. The collector of Q28 is at a + voltage set by the divider R2 and R21. When the range ramp runs up to one junction drop more positive than the zener diode CR6, Q27 conducts as a grounded base amplifier and the delay ramp is clamped at this voltage for the remainder of the first half of the 1 ms hold-off interval. Collector current from Q27 provides enough base current to saturate Q28. The resulting negative-going collector waveform of Q28 provides the drive to increase the digital counter by 1 bit.

n. BCD Counter. The BCD (binary coded decimal) counter is a synchronous counter made up of integrated circuit J K flip-flops and logic gates. The input to the counter is the waveform from the counter driver which increases the counter by one bit at the end of each range ramp. The output of the counter is 12 diode-isolated logic lines with conventional 1-2-4-8 BCD logic. That is, when the counter is in the "0" state, all logic lines are 0 V. Logic "1" is +3 V.

Twelve J K flip-flops are used, 2 contained in each of 6 IC packages (IC 10 through IC 15). The remaining packages on the board, IC 1 through IC 9, are logic gates.

The operational characteristics of the J K flip-flops are: (1) if the S/C inputs are at 0 V when a bit is applied to the T input, the flip-flop will change states; and (2) if the S/C inputs are + when the bit is applied to the T input, the flip-flop will not change states.

The operational characteristics of the logic gates are: (1) if any input to a single gate is +, the output will be 0, and (2) if all inputs to a single gate are 0, the output will be +.

The input bit from the counter driver is applied to the T input of all 12 flip-flops in parallel. The logic gates controlling the S/C inputs determine whether or not a particular flip-flip will accept the trigger and change states.

Two fundamental requirements of a binary counter are: (1) the low order stage must change states with each input bit, and (2) each of the remaining stages must change states when all lower order states are changing from "1" to "0". In addition to these fundamental binary requirements, if the output is to be BCD, all stages within a single decade must be in the "0" state as a result of the 10th input bit.

The first binary requirement is met by simply grounding the S/C inputs on the first stage. The S/C inputs of the first stage are always 0 V, and the first stage will change states with each input bit.

The second binary requirements (all remaining stages change states when all lower order stages switch from "1" to "0") is met by making the S/C inputs of each stage an AND term of the Q output of all lower order stages. Therefore, an input bit can switch the state of a stage only if all lower order stages are "1" when the input bit is applied.

The third requirement (to make the full decade "0" as a result of the 10th bit) is accomplished by inhibiting the "2" stage and forcing the "9" stage on the 10th input. The "1" stage normally goes to "0" on the 10th input bit, so no extra influence is needed. The "2" stage is at "0" after the 9th input bit, but it will normally switch on the 10th bit if not prevented. The "4" stage is at "0" after the 9th bit and will normally stay at "0" after the 10th bit, so no additional influence is needed. The "8" stage is at a logic "1" after the 9th bit, and will not normally revert to "0" until the 16th bit. The "8" stage must be switched to "0" by the 10th input bit.

The logic levels in Fig. 3-1 show the output voltage levels from each stage in the first decade of count.

The S/C inputs to the low order stage, pins 7 and 5 of IC 10A, are permanently grounded. Therefore the low order stage switches states on each input bit.

The logic at the S/C input to the remainder of the stages is an AND term of the Q output of all lower order stages. Any stage can switch states on an input bit if all lower order stages are a logic "1" when the input bit is applied.

The output of the logic gate 1C is up if the first decade is "9" (simultaneously "1" and "8"). This output inhibits the 2nd stage from switching and permits the 8th stage to switch on the 10th input bit, thus causing the first decade to assume the "0" state after the 10th input bit.

The second decade functions the same as the first decade except the logic gate 1D inhibits the entire second decade on all input bits except the first decade overflow bits.

Similarly the third decade functions the same as the first two except that the logic gates 3A and 3B inhibit the third decade on all bits except the second decade overflow bits.

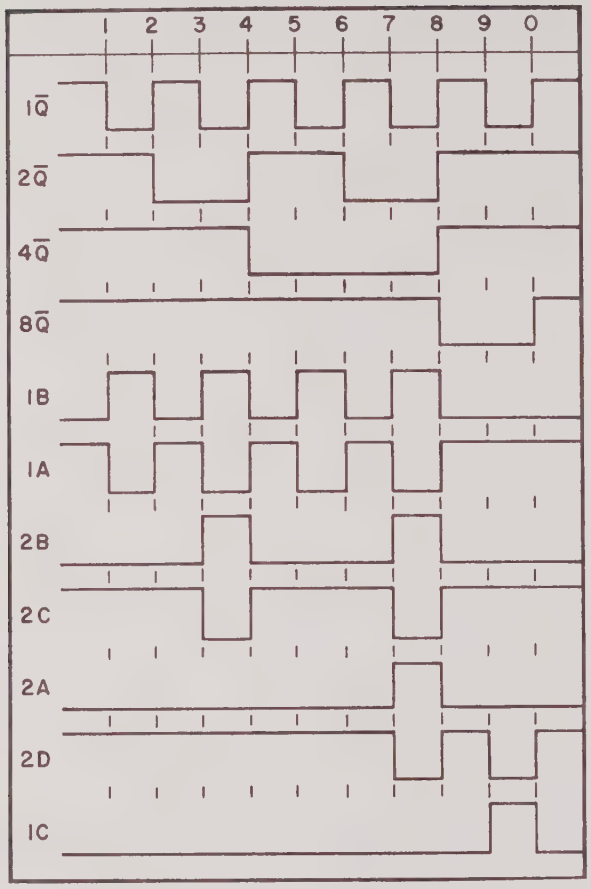

Figure 3-1 Logic Levels In The BCD Counter

There are 12 output transistors, Q1 through Q12. Each of the output transistors drives one of the logic lines. The Q output of each counting stage provides base current for its respective output transistor when that stage is in the "0" state. When an output transistor is conducting, its collector is clamped near ground. When the counting stage is in the "1" state, no base current is supplied by the Q output, and the output collector goes positive to the power supply voltage. Therefore the 12 logic lines carry true BCD logic. That is, logic "1" is +3 V, and logic "0" is 0 V.

o. **D/A Converter.** The D/A converter is a 3-decade digital-to analog converter. The inputs to the D/A converter are the 12 BCD logic lines from the digital counter or from the external programming connector, J302. The output of the D/A converter is a voltage between 0 and +5 V proportional to the value of the number represented by the BCD code.

The D/A converter is made up of 12 saturating switches, each with a current weighting resistor proportional to the numerical value of its logic line, and a common current-summing output stage.

Since the 12 saturating switches are identical, except for the value of the current weighting resistor, only the "1" switch will be discussed. The "1" saturating switch consists of Q39, Q38 and their associated components. If the "1" logic line is down (0 V) neither Q39 nor Q38 have base current, and neither conducts. If the "1" logic line is up (+3 V), Q39 conducts supplying base current to Q38. Q38 saturates, and collector current is determined by the value of R37, the current weighting resistor. Each of the 12 saturating switches provides current to the output stage proportional to the numeric value of its logic line.

The output stage, Q4, is a grounded base amplifier. Emitter current for Q4 is the sum of the 12 weighted currents plus a constant idling current supplied through R12 and R13 from the +15 V supply. The collector load for Q4 is R6 and R7 on the buffer board. The collector is returned to a Thevenin-equivalent of -0.25 V to compensate for the effect of the idling current.

The D/A converter board may be rewired to latch and hold, or to accommodate other than 1-2-4-8 BCD logic. Contact your E-H Representative or the factory for exact details.

p. **Strobe Generator.** The strobe generator gates the sampling bridge on during the first 4 ns of the delayed pulse. The strobe generator consists of Q6, Q7, Q8, Q9, Q10, Q11 and the pulse transformer T1. In the quiescent condition, each of the three pairs have one transistor conducting and the other turned off. Q7 is conducting because of the dc level provided to its base by the delayed pulse generator. Q6 is turned off. The clip line is a dc short-circuit between the collectors of Q6 and Q7. The junction drop across CR5 holds the base of Q8 one junction drop more negative than the base of Q9, therefore Q9 conducts and Q8 is turned off. Q9 provides base current to Q11, so Q11 conducts and Q10 is turned off.

The timing element in the strobe generator is the clip line connected between the collectors of Q6 and Q7. In the quiescent condition, R48 and R50 are parallel collector loads to Q7 with the current through R50 flowing through the clip line. When the delayed pulse switches current from Q7 to Q6, R48 and R50 are parallel collector loads to Q6 with current from R48 flowing through the clip line. When Q6 is conducting, current flow through the clip line is in the opposite direction from the quiescent condition. During the 4 ns required to discharge the clip line and charge it back in the opposite direction, the surge impedance of the clip line can be considered as two 50-ohm resistors; one from the collector of Q6 to ground, the other from the collector of Q7, to ground. After the 4 ns transistion time, the clip line is again a dc short-circuit between the collector of Q6 and Q7.

The leading edge of the positive-going delayed pulse turns off Q7 and turns on Q6. For 4 ns following current-switching, Q6 and Q7 each have an effective collector impedance of 25-ohm. When the 30 mA through R51 is switched from Q7 to Q6, the collector of Q7 goes negative 0.75 V and the collector of Q6 goes positive 0.75 V. These voltages cause Q8 to conduct and Q9 to turn off. Current is switched from Q11 to Q10 and the current flow through the primary of T1 is reversed for 4 ns. The output pulse from T1 gates on the sampling bridge.

The voltage divider made up of R23, R22, R21, R20 and R19 provides back bias for the sampling bridge diodes. For proper adjustment of R23, refer to the calibration procedure in Section 4.

q. **DC Offset Amplifier.** The dc offset amplifier provides the reference level for the sampling bridge and the first memory amplifier. The measurement made by the Model 153, is the voltage difference between the input signal at

strobe time and the dc offset voltage. The output of the dc offset amplifier is equal to the externally applied dc offset input between the limits of -1 V and +1 V.

The dc offset amplifier is a voltage-feedback stabilized amplifier made up of Q15A, Q15B, Q12, Q13 and Q14. The dc offset input is applied to the base of Q15A. Q15A and Q15B are connected as a voltage-amplitude discriminator pair. They share a common source of emitter current through R25 from the -15 V supply. Q15A provides base current to Q14, Q15B provides base current to Q12, and Q12 in turn drives Q13. The phase relationship through the amplifier is such that the collector current of Q13 pulls the base voltage of Q15B up to equal the voltage at the base of Q15A. The current flow through R36 and R35 necessary to hold the base of Q15B equal to the base of Q15A must also flow through R34. The dc voltage at the collector of Q13 is 1.3 times the dc voltage at the base of Q15B. The voltage at the collector of Q13 provides the reference level for the feedback resistors in the first memory amplifier. The voltage at the base of Q15B provides the reference voltage for the sampling bridge through R2.

r. First Memory Amplifier. The first memory amplifier is a high-input-impedance operational amplifier with a voltage gain of 4X. At the end of the programmed delay interval, the sampling bridge is turned on for 4 ns, connecting the applied signal to the input of the first memory amplifier. The input time-constant, while the sampling bridge is turned on, is approximately 0.5 ns. This time-constant, together with the 4 ns strobe width, permits C1 to charge to the full signal voltage present on the bridge at the end of strobe time. After strobe time, when the input to the first memory amplifier is isolated from the signal source, the input time-constant is about 50 μs.

The first memory amplifier is made up of Q1A, Q1B, Q2, Q3A, Q3B, Q4 and Q5. The signal input is at the gate of Q1A. The feedback voltage is applied from the output through the voltage divider, R16-R32, to the gate of Q1B. Within the voltage-gain limitations of the amplifier, the voltage at the gate of Q1B is held equal to the voltage at the gate of Q1A. The amplifier has a voltage gain of 4X set by the ratio of R32 to R16 + R32.

When a dc offset voltage is applied to the input of the first memory amplifier at the gate of Q1A, an equal dc offset must be applied to the gate of Q1B so the output of the first memory amplifier will be 0 V with no input signal applied. The ratio of R16 to R32 dictates that the voltage applied to the bottom of R32 must be 1.3 times the voltage applied to the gate of Q1B. Since it is desirable for the voltage at the gate of Q1B to equal the voltage at the gate of Q1A, the voltage gain of the dc offset amplifier must be 1.3. The feedback divider, R16 and R32, are referenced to a point in the dc offset amplifier which is 1.3 times the dc offset voltage.

s. Strobe Time Trigger Generator. The strobe time trigger generator buffers the delayed pulse signal to drive the memory gate generator, and the data record delay generator and provide the Strobe Time Trigger Output.

Q14 and Q15 form a current mode switching pair whose bases are biased by matched zener diodes. The base of Q15 is quiescently more positive than that of Q14, except during the delayed pulse when it is driven more negative than Q15. This results in a voltage waveform on the collector of Q14 which is in phase with the delayed pulse (i.e., negative going pulse) and a waveform on the collector of Q15 which is out of phase (i.e., positive going). Q16 emitter follows the positive going waveform to the Strobe Time Trigger Output connector.

t. Memory Gate Generator. The memory gate generator is a one-shot multivibrator which is triggered at the trailing edge of the delayed pulse (by way of the Strobe Time Trigger Generator). It generates a 1.2 μs gate which turns on the memory gate bridge. By starting the memory gate from the trailing edge rather than the leading edge of the delayed pulse, the first memory amplified is allowed 200 ns to reach its peak amplitude before the second memory amplifier samples its output.

The one-shot multivibrator is Q12 and Q13. Q10 and Q11 make up a current-switching output stage. In the quiescent condition, Q13 is on and saturated because of the current flow through R49 and R51. Q12 is then not conducting, there being no bias current available to turn the base on. The quiescent state for the current mode pair, then, is for Q10 to be conducting and Q11 off, because the base of Q10 is more positive than that of Q11.

At the trailing edge of the delayed pulse, the collector of Q14 goes positive. This signal is coupled through C8 and CR5 to turn Q13 off, which causes Q12 to go on into saturation. Q13 is then held off by the charge on C7 which holds the base of Q13 positive after the trigger pulse terminates. The current through R49 and R51 eventually discharges C7 and turns Q13 on again, which in turn drives Q12 off. The period of the multivibrator is determined by the time constant of C7, R49 and R51.

During the 1.2 μs that Q13 is off and Q12 on, the states of Q10 and Q11 reverse, as their bases follow the voltages on Q13 and Q12. The change in collector current of Q10 and Q11 is coupled through the pulse transformer, T1, to turn on the memory gate bridge for 1.2 μs.

u. Memory Gate Bridge. The memory gate bridge (CR1A, CR1B, CR1C and CR1D) connects the output of the first memory amplifier to the input of the second memory amplifier for 1.2 μs starting 200 ns after strobe time.

v. Second Memory Amplifier. The second memory amplifier is a high-input-impedance operational amplifier with a voltage gain of 2.5X. It follows the voltage on the memory capacitor C_2 which at the end of the memory gate is 4 times the measured input voltage.

The second memory amplifier is made up of Q1A, Q1B, Q2, Q3A, Q3B, Q4 and Q5. The signal input is at the gate of Q1A. The feedback voltage is applied from the output through the divider (R18-R19-R20) to the gate of Q1B. Within the open-loop voltage gain limitations of the amplifier, the voltage at the gate of Q1B is held equal to the voltage at the gate of Q1A. The voltage gain of the amplifier is set by the ratio of R19 + R20 + R18 to R19 + R20. The holding time-constant of 250 ms is set by the input capacitor, C2, and the input resistor, R3 through R7.

w. Output Amplifier. The output amplifier includes the OUTPUT GAIN selector switch, S202, and an operational amplifier with a voltage gain of 10X. The operational amplifier is made up of Q6, Q7, Q8 and Q9.

When the OUTPUT GAIN selector switch is in the X1 position, the output of the second memory amplifier is attenuated by a factor of ten by the voltage divider, R23-R201-R202. The 10X voltage gain of the memory amplifiers together with the 10X attenuation at the output makes the voltage available at the output connector,V(t), equal to the applied signal voltage at strobe time.

When the OUTPUT GAIN selector switch is in the X10 position, the output of the second memory amplifier is connected directly to the output connector, V(t). The voltage gain of the memory amplifiers provides the overall voltage gain of 10X.

When the OUTPUT GAIN selector switch is in the X100 position, the output of the second memory amplifier drives the input of the output amplifier, and the output amplifier drives the V(t) output connector.

The input to the operational amplifier is the base of Q6. The feedback voltage is applied from the output through the divider, R33-R34, to the base of Q7. The voltage gain of the operational amplifier is set by the ratio R34 to R33 + R34.

x. **Data Record Delay Generator.** The Data Record Delay Generator is a one-shot multivibrator made up of Q17 and Q18. It is triggered at the trailing edge of the delayed pulse waveform by the Strobe Time Trigger Generator and drives the data record trigger generator. The purpose of the 2.5 μsec delay iis to permit risetimes through the memory amplifiers before signaling auxiliary equipment that the output voltage is ready for use.

In the quiescent condition, Q17 conducts at saturation, holding its collector near ground. Q18 does not conduct since it has no source of base current. The negative-going 200 ns pulse at the collector of Q14 is differentiated by C10 and R63. The positive-going spike at the end of the pulse is coupled through CR7 and turns off Q17. The negative-going waveform at the collector of Q17 provides base current to Q18 through R69. Q18 saturates and pulls its collector voltage up to ground. The positive-going waveform at the collector of Q18 is coupled to the base of Q17 through C16. Q17 remains turned off for 2.5 μs determined by the time-constant of C16 and R65. When C16 has discharged far enough for the base of Q17 to go one junction drop below ground, Q17 goes back into conduction and pulls its collector back up to ground. When the collector of Q17 returns to ground, Q18 turns off and the one-shot multivibrator returns to its quiescent condition.

y. **Data Record Trigger Generator.** The data record trigger generator is a one-shot multivibrator, Q19 and Q20, buffered to the connector through an inverter, Q21. This one-shot is triggered by the trailing edge of 2.5 μs delay and has a period of about 1.7 μs.

Operation of this one-shot is identical to that of the above delay one-shot. Q19 gets driven off through C12 and CR8 when Q17 turns on at the end of the 2.5 μs delay interval. The collector of Q19, which goes negative during the one-shot period, drives Q21 off for the duration of the one-shot period. This allows the collector of Q21 to go positive during the data record trigger period.

z. **Regulated Power Supplies.** Five regulated power supplies provide operating voltages to the circuitry in the Model 153.

The +25V regulated power supply is made up of Q1, Q2, Q3, Q101 and the zener reference CR5. Q1 and Q2 are a voltage-amplitude comparator pair, Q3 provides open-loop voltage gain, and Q101 is the series regulating element. The voltage at the base of Q1 is held to +9.0 V by the zener reference, CR5. A proportional sample of the +25 V supply is applied to the base of Q2 through the divider, R5-R6-R7. The phase relation through the amplifier is such that the output at the emitter of Q101 is out of phase with the error voltage at the base of Q2. The open-loop gain of the amplifier holds the output voltage at the +25 V buss to whatever voltage is necessary to minimize the error voltage at the base of Q2.

The +15 V regulated supply is made up of Q7, Q8, Q9, Q103 and the zener reference CR5. With the exception of the component values, the +15 V supply functions in the same manner as the +25 V supply described above.

The -15 V supply is made up of Q10, Q11, Q12 and Q104. Q10 and Q11 are the voltage-amplitude discriminator pair, Q12 provides open-loop gain, and Q104 is the series regulating element. The base of Q10 is referenced to ground. Since R27 and R28 are equal values, the -15 V supply must be as much negative as the +15 V supply is positive to provide the base of Q11 with a voltage equal to the base of Q10. The open-loop gain of the amplifier pulls the voltage at the emitter of Q104 in the direction that will minimize the error voltage between the base of Q11 and the base of Q10. The exact voltage output of the -15 V supply is dependent on the output of the +15 V supply.

The -25 V supply is made up of Q4, Q5, Q6 and Q102. Q4 and Q5 are the voltage-amplitude discriminator pair, Q6 provides open-loop gain, and Q102 is the series regulating element. The base of Q4 is referenced to ground. The voltage at the base of Q5 is established by the divider, R12-R13 between the +25 V supply and the output of the -25 V supply. As with the -15 V supply discussed above, regulation of the -25 V supply depends on regulation of the +25 V supply.

The +3.6 V supply is made up of Q13, Q105 and the zener reference CR6. CR6 provides the reference voltage, Q13 is the voltage comparator and provides the open-loop gain, and Q105 is the series regulating element. The base of Q14 is held at +4.3 V by the zener reference CR6. Collector current from Q13 provides base current for Q105. As the collector of Q105 pulls positive, it robs current from the emitter of Q13, one junction drop below the zener reference voltage.

SECTION 4
MAINTENANCE

4-1 GENERAL

The E-H Model 153 Strobing Voltmeter requies a minimum amount of maintenance; however, normal aging of electronic components may eventually cause abnormal operation. Therefore, general maintenance and trouble shooting information is included in this section as a guide to restoring the instrument to normal operation.

4-2 ROUTINE MAINTENANCE

A regular program for maintenance and inspection every four to six months is recommended to effectively minimize equipment down time. As part of the regular maintenance and inspection procedure, the instrument should be carefully checked in the following manner:

a. Remove the Model 153 cover panels.

b. Make a thorough inspection of all wiring and cables. Check for frayed, loose or burned wires.

c. Check the physical integrity of all components. Look for evidence of burning or cracking, loose solder connections, leakage of insulation compounds and general physical damage.

d. Check all switches and controls for loose or broken terminals, tight or sticking shafts, etc.

e. If the internal panel surfaces and components have an excessive amount of dust or lint deposited on them, use a low pressure stream of air to remove the foreign material.

CAUTION

Do not clean the circuit boards or small internal components with a wiping cloth or solvents, since damage to the circuits may result.

f. Wipe the external surfaces of the instrument with a soft, damp cloth to remove dirt, fingerprints, and other foreign materials.

g. Remove and clean the metal air filter. The filter may be washed in soapy water. Rinse in clear water, dry and replace the filter on the instrument. The filter must be kept clean and unrestricted.

h. If repairs are made to the instrument, or if a performance verification indicates that it is not operating within the tolerances stated in Section 1, a complete calibration procedure as outlined in this section should be performed. Before attempting the calibration procedure, read Section 3 of this instruction manual. A working knowledge of the circuitry is necessary to insure optimum performance of the instrument.

4-3 CALIBRATION PROCEDURE

a. Equipment required.

(1) Time mark generator - Tektronix Type 184 or equal.

(2) Real time oscilloscope - Tektronix Type 547 or equal with a differential (type W) plug-in.

(3) Voltmeter 1% accuracy - Simpson 262 or equal.

(4) Resistors 1/2 watt, 5%; 30 k, 3 k, 270Ω.

(5) Pulse Generator, E-H Model 139B or equal.

b. Precautions. Component density on the etched circuit boards is high. Leads are close together and one side of the circuit board is a ground plane. Take care, when attaching voltmeter leads, oscilloscope probes, etc. that the probe touches only the point to be tested. Solid state junctions can easily be destroyed by allowing the test lead to touch two points or one point and ground.

For best results, it is recommended that the entire calibration procedure be performed in the sequence stated.

c. Adjust and Check regulated supplies.

(1) Measure the +15 V supply at pin 6 of the printed circuit board sockets, and adjust R20, "+15 V adj", for +15 V±1%.

(2) Measure the +25 V supply at pin 15 of the printed circuit board sockets, and adjust R6, "+25 V adj", for +25 V ±1%.

(3) Check the -15 V supply at pin 7 for -15 V ±3%.

(4) Check the -25 V supply at pin 14 for -25 V ±3%.

(5) Check the +3.6 V supply at pin 1 of the regulator board socket for +3.6 V ±10%.

d. Adjust delay analog buffer.

(1) With the DELAY MULT. SOURCE switch on Analog/INT, and the DELAY MULTIPLIER set to 10.00 (not full clock-wise), measure the voltage at pin 9 of the buffer board socket, J104. Adjust R2, "Multi pot cal", for +5 V ±0.01 V. Make this adjustment carefully, it is the reference for the delay timing.

(2) With the DELAY MULT. SOURCE switch on ANALOG/INT, and the DELAY MULTIPLIER set to 0.50, check the voltage at pin 9 of the buffer board socket, J104. Voltage must be between 0.25 V and 0.27 V. If this voltage is incorrect, select R4 on the buffer board. If R4 is changed, repeat step (1).

(3) With the MULT. SOURCE switch on ANALOG/EXT and the DELAY ANALOG IN connector (304) grounded, measure the voltage at the DELAY

ANALOG OUT connector (302). Adjust R13, "zero", on the buffer board for 0 V. Final adjustment should be made with the meter on a current scale that is capable of resolving 10 μa.

(4) With the MULT. SOURCE switch on ANALOG/INT, and the DELAY MULTIPLIER set to 10.00, measure the voltage at the DELAY ANALOG OUT connector, J303. This output has a source impedance of 1 kilohm which must be considered if the impedance of the measurement device is less than 1 megohm. The output voltage should be +10 V ±2%.

e. Adjust incremental delay range accuracy.

(1) Use the test set-up shown in Fig. 4-2. Trigger the Model 153 with the 1 msec markers. Calibrate the horizontal input of the test oscilloscope with the DELAY MULT. SOURCE switch on ANALOG/INT. Set the DELAY MULTIPLIER to 1.00 and adjust the horizontal positioning so the spot is 1 cm from the left edge of the graticule. Set the DELAY MULTIPLIER to 10.00 and adjust the horizontal input sensitivity so the dot is 10 cm from the left edge of the graticule. Repeat these two adjustments until there is no further interaction.

With the test scope in the external-horizontal input mode, free-run the sweep at 100 msec/cm (1 sec total sweep time) and select the resistor between the sawtooth output and the DELAY ANALOG IN for 10.5 cm of horizontal deflection (approximately 30 kilohm).

Make the above test set-up carefully. It is desirable to read the horizontal axis of the oscilloscope display to better than 1%.

(2) Display the 0.1 μs markers on the 1 μs DELAY RANGE. Adjust the horizontal positioning of the test oscilloscope and R16, "scale", on the buffer board so the last 9 markers coincide with major graticule marks on the test oscilloscope. Check the 10 μs range using 1 μs markers, and the 100 μs range using 10 μs markers in the same fashion. Compromise the adjustment of R16, "scale", for best accuracy of all three ranges. "Worst case" range should be within 2%.

(3) Display a 10 MHz sine wave on the 100 ns delay range, and adjust C19 on the trigger board so the last 9 cycles coincide with the major graticule marks within 1%.

(4) After adjusting the horizontal positioning of the test oscilloscope so each marker coincides with major graticule marks, switch the DELAY MULT. SOURCE switch to INT. Set the DELAY MULTIPLIER to the peak of the marker which is 1 cm from the left edge of the graticule and then to the peak of the marker which is 10 cm from the left edge of the graticule. The difference between the two settings must be between 8.91 and 9.09.

(5) Repeat step (4) on each of the other 3 DELAY RANGES, using 1/10th full scale markers on each range. On the 1 μs, 10 μs, and 100 μs ranges, the difference between the two settings must be between 8.82 and 9.18.

f. Adjust delay range offset.

(1) With the test set-up described in c. above, display the 20 MHz sine wave (50 ns) on the 100 ns delay range. Check the horizontal calibration of the test oscilloscope; that is, the spot under the 1 cm graticule mark when the DELAY MULTIPLIER is set to 1.00 and under the 10 cm mark when the DELAY MULTIPLIER is set to 10.00.

With the DELAY MULT. SOURCE on ANALOG/EXT, observe the point on the 20 MHz sine wave at the 10 cm graticule mark. Switch to the 1 μs DELAY RANGE, and adjust R20, "offset", on the buffer board so the same point

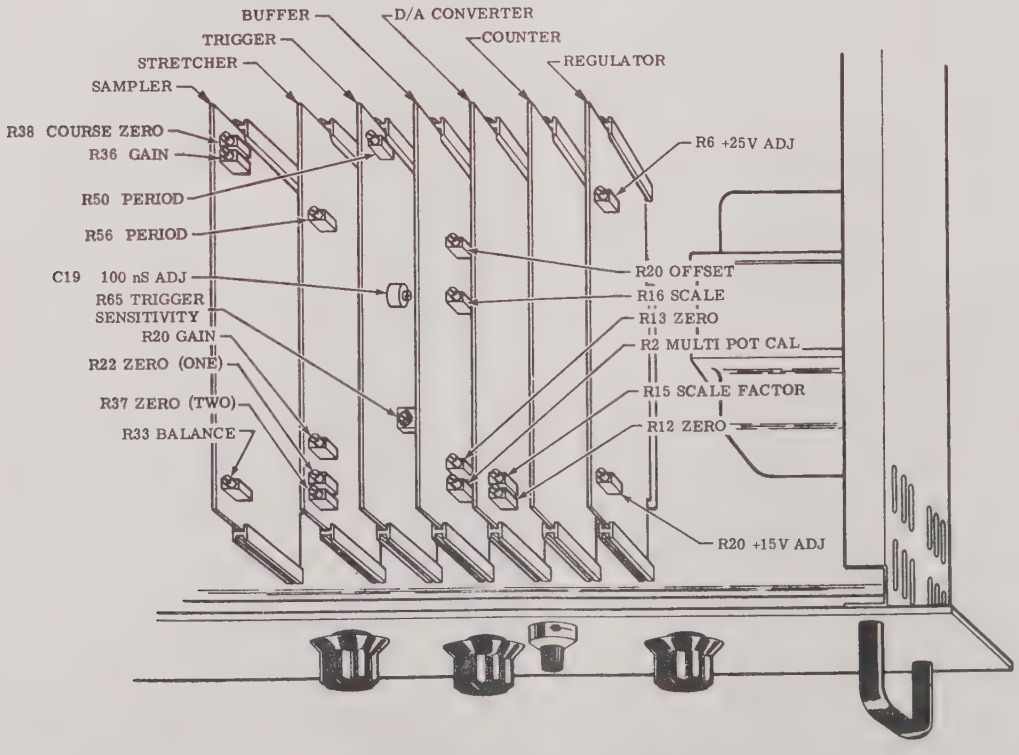

Figure 4-1 Location of Calibration Adjustments

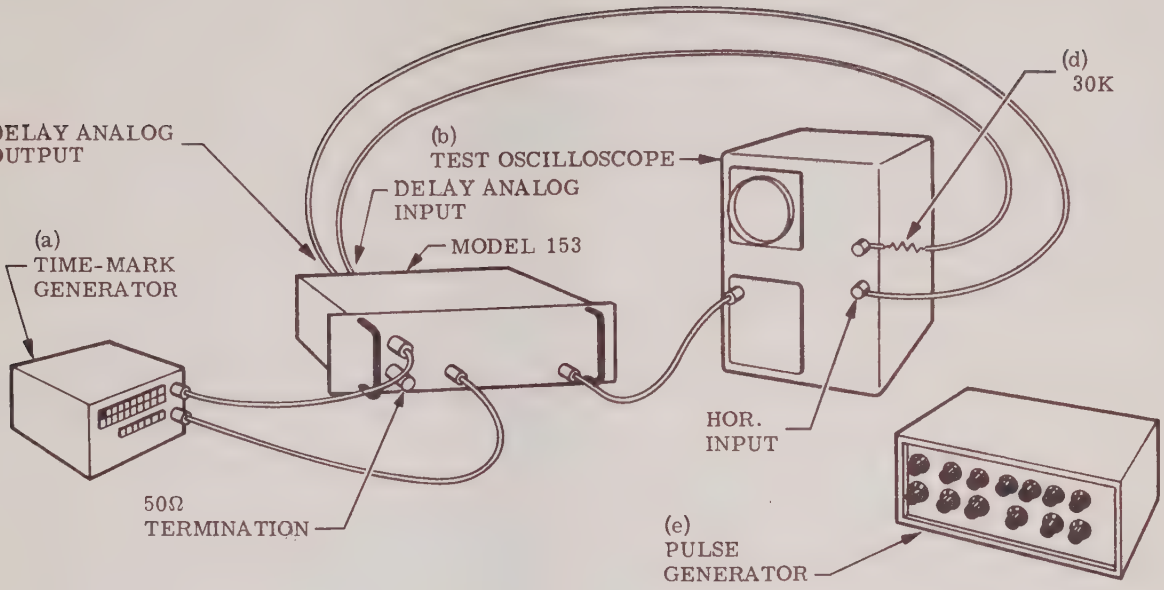

Figure 4-2 Basic Test Set-up For Calibrating Incremental Delay Range Accuracy

on the 20 MHz sine wave coincides with the 1 cm graticule mark. Switch back and forth between the 100 ns DELAY RANGE and the 1 μs DELAY RANGE while making the adjustment.

Display the 0.5 μs markers using the 1 μs DELAY RANGES as stated above.

Display the 5 μs markers using the 10 μs and the 100 μs DELAY RANGES as above. Adjust R20, "offset", for the best compromise among all ranges.

g. Adjust Internal Timing Waveforms.

(1) Trigger the Model 153 and the test oscilloscope with the 1 msec trigger output from the time-mark generator. Set the DELAY RANGE to 100 ns and the MULTI SOURCE to ANALOG/INT.

(2) Display the waveform at pin 22 of the trigger board socket, J103, on a 200 ns/cm sweep. Adjust R50 "period" on the trigger board so that the period of the observed pulse is 200 ns. This is referred to as the delayed pulse. It is a negative pulse with its base line above ground, and its pulse top below ground.

(3) Switch the test oscilloscope to the 1 μs/cm sweep speed and observe the position of the leading edge of the delayed pulse (the negative pulse at pin 22, J103). Without disturbing the test scope, observe the waveform at pin 20 of the stretcher board socket, J102. The waveform should not be less than 1.2 μs wide, approximately 2.5 μs after strobe time.

(4) Display the waveform at the collector of Q13 on the Stretcher Board at 500 ns/cm. The observed pulse has the same width as the Memory Gate Pulse. Adjust R51, "period", on the stretcher board for a 1.2 μs memory gate pulse width.

h. Adjust Sampler Bridge Balance.

(1) Without triggering, and with no signal input, adjust R23, "balanced" on the sampler board for equal + and bias voltage on the sampling bridge. The bridge bias voltages may be measured at the terminals of T1 on the sampler board. The + and - bias voltages should be equal in amplitude and between 0.88 V and 0.95 V.

i. Adjust Transfer Offset.

(1) Trigger the test oscilloscope and the Model 153 with the 1 ms trigger output from the time marker generator. Set the DELAY RANGE to 100 ns and the MULTI SOURCE to ANALOG/INT.

(2) Display V(t) output at 1 μs/cm with the OUTPUT GAIN at X10. Short the output of the sampler board (pin 16) to ground (pin 17) with a short jumper. Adjust R22 "zero 1" on the stretcher board so that the V(t) output is 0 V ±1 mV at a point 3 μs after the trigger pulse.

(3) Switch the OUTPUT GAIN control o X100. Wait one minute to allow the X10 amplifier to thermally stabilize. Adjust R37, "zero 2", on the stretcher board so that the V(t) output is 0 V ±10 mV 3 μs after the trigger pulse.

(4) Return the OUTPUT GAIN Control to X10, remove the jumper across pin 16 and 17 of the sampler board. Preset the rear mounted ZERO control to mid-range. Terminate the SIGNAL IN and SIGNAL OUT connectors on the Model 153 in 50-ohm to ground. Adjust R38, "zero", on the sampler board so that the V(t) output (which is smeared out because of sampling noise) has an average value of 0V at 3 μs after the trigger pulse.

(5) Set the OUTPUT GAIN TO X1. Monitor the output voltage at V(t). Remove the trigger. The output voltage should remain within ±20 mV of O V (±20 μA if the output is being monitored with a microammeter).

j. Adjust the transfer gain.

(1) Pad down the X output of the oscilloscope's horizontal sweep as shown to provide a sweep from -1.0 V to +1.0 V. Adjust R_A and R_B as necessary so that the pad's

output swings equally around 0 V and >1 V. C_A may be necessary to minimize the noise picked up by the lead to the -15 V supply. The cables attached to the SIGNAL IN and SIGNAL OUT connectors must be high quality 50-ohm with coaxial connectors and be >1 ns long so that the sampling bridge sees a constant (50-ohm) impedance for the duration of the strobe pulse. (The internal cable contributes ~3 ns so the round trip time for the two together is >4 ns which is the strobe width. Connect this signal to the Model 153 SIGNAL IN and the SIGNAL OUT to the (-) input of the differential plug in. Set the Model 153 OUTPUT GAIN to X1, and connect the V(t) output to the (+) input of the differential plug-in. Trigger the Model 153 with the 1 ms trigger from the time marker generator, and free run the oscilloscope at 0.2 sec/cm.

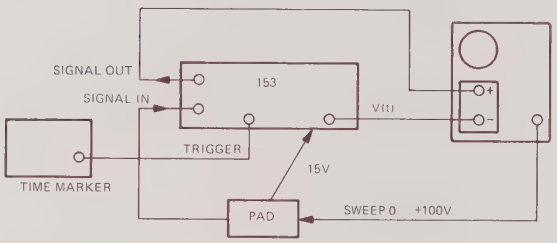

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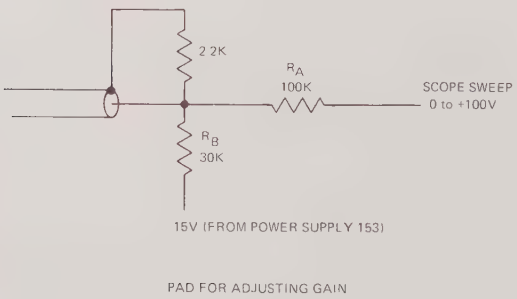
Figure 4-3 Gain Adjustment Test Set-up



EH-L0417

Figure 4-4 Gain Adjustment Schematic

(2) Observe the differential voltage between the input and the output of the Model 153. The trace is not a clean line for three reasons: (1) sampling noise and stray pick up in the measurement lead (2) discharging of the Model 153's memory between samples and (3) difference in the input and the output of the Model 153 between samples (the input is a smooth ramp while the output is a staircase). Because of 2 and 3 above, the input and output are only equal immediately after a sample. In interpreting the above display, then, the lower side of the envelope should be read on the left hand side and the upper side of the envelope on the right. Adjust R20 "gain" on the stretcher board so that the corrected waveform falls within the superimposed ±10 mV (±1% error) guide lines.

(3) Trigger the Model 153 at 1 kHz. Connect an open 50-ohm cable, not less that 2 ns in length, to the SIGNAL IN connector. Connect the SIGNAL OUT connector to the OFFSET INPUT connector. Set the OUTPUT GAIN to X1 and alternately apply +1 V and -1 V to the SIGNAL INPUT, and adjust R36 "gain" on the sampler board, for less that 4 mV output at V(t). The +1 V and -1 V can be accomplished by connecting a 1.5 k resistor between the paralleled inputs and the + or -15 V supplies.

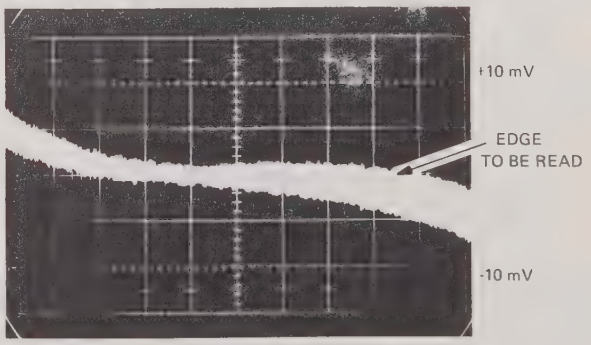
k. D/A calibration (if D/A card is installed.)

(1) Set DELAY MULTI. SOURCE to DIGITAL/EXT. Monitor the voltage output at the DELAY ANALOG OUT connector, J303. Adjust R12, "zero adjust", on the D/A board for 0 V output.

(2) Set the DELAY MULT. SOURCE to DIGITAL/AUTO STEP. Display a 2 MHz sine wave (50 ns) on the 1 μs delay range, using the test set-up shown in Figure 4-2. Set the DELAY MULTIPLIER to 10.00. Switch the DELAY MULT. SOURCE alternately from DIGITAL/AUTO STEP to ANALOG/INT. Adjust R15, "scale factor", on the D/A board so the maximum delay from the D/A board is equal to the INT. delay.

l. Trigger Adjustment

(1) Connect the test oscilloscope as shown in Figure 4-2. Drive the SIGNAL IN from a variable-amplitude 50-ohm pulse generator. Connect the SIGNAL OUT to the TRIGGER IN. Set TRIGGER SENSITIVITY fully counter-clockwise. Adjust the amplitude of the pulse generator and determine the minimum amplitude for triggering. Adjust R65, "trigger sensitivity", on the trigger board for a triggering threshold between 90 mV and 100 mV.



EH-0149

Figure 4-5 Trace of Differential Voltage

SECTION 5
PARTS LIST

5-1 ORDERING INFORMATION

Replacement parts may be ordered through an E-H Representative or directly from the factory. To be certain of receiving the proper parts, always include the following information with the order:

a,, Model number and serial number of the instrument on which the parts will be installed.

b. Circuit reference number and subassembly name, if applicable, for which the part is intended. If the part does not have a circuit reference, the description from the parts list should be used.

c. E-H part number.

The warranty and instructions for in-warranty repair of this instrument are given on page ii of this manual, opposite the Table of Contents. For factory repair, contact the Customer Service Department of E-H Research Laboratories, Inc., at the address given on the title page of this manual. Include the following information:

a. Model number and serial number of the instrument on which the work is to be performed.

b. Details concerning the nature of the malfunction; or, type of repair desired.

Shipping instructions will be sent to you promptly.

5-2 HOW TO USE THIS PARTS LIST

The parts list is divided into subsections corresponding to the physical subsections of the instrument (printed circuit boards, chassis and subassemblies, miscellaneous hardware). Component locations can be determined from the schematic diagrams in the Appendix; each component appears only once in the parts list. At the beginning of each subsection are listed part numbers for any complete subassemblies in that category that are available as replacement parts. These subassemblies may include individually-listed components; care should be taken to locate malfunctions to the lowest possible level of replacement part and thus avoid the time and cost involved in "over-repair".

5-3 SAMPLER BOARD

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
C1	Cap., 10pF	311-00051
C2	Cap., .001μF	311-00016
C3	Cap., 1.0μF, 25V	311-00038
C4	Cap., 75pF	311-00025
C5	Cap., .002μF	311-00017
C6	Cap., 1.0μF, 25V	311-00038
C7	Cap., 1.0μF, 25V	311-00038
C8	Cap., .01μF	311-00012
C9	Cap., .1μF, 50V	311-00034
C10	Cap., 25 μF, 25V	316-00028
C11	Cap., 1.0μF, 25V	311-00038
C12	Cap., .1μF, 50V	311-00034
C13	Same as C10	
C14	Same as C11	
CR1A	Diode	376-11758
CR1B	Same as CR1A	
CR1C	Same as CR1A	
CR1D	Same as CR1A	
CR2	Diode, zener	374-12529
CR3	Same as CR2	
CR4	Same as CR2	
CR5	Diode, 1N924B	376-00022
CR6	Same as CR2	
Q1A	Transistor	663-00092
Q1B	Transistor	663-00029
Q2	Transistor	663-11749
Q3A	Transistor	663-11759
Q3B	Same as Q3A	
Q4	Same as Q2	
Q5	Transistor, 2N3251	663-00076
Q6	Transistor	663-11757
Q7	Same as Q6	
Q8	Transistor	663-11722
Q9	Same as Q8	
Q10	Transistor	663-11770
Q11	Same as Q10	
Q12	Transistor, 2N3906	663-00071
Q13	Same as Q2	
Q14	Transistor, 2N3906	663-00071
Q15A	Transistor	663-11748
Q15B	Same as Q15A	

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
R1	Resistor, 10K, 1/4W, 5%	595-00103
R2	Resistor, 5.1M, 1/4W, 5%	595-00515
R3	Resistor, 10K, 1/4W, 1%	617-00012
R4	Resistor, 2K, 1/4W, 5%	595-00202
R5	Resistor, 51 Ω,1/4W, 5%	595-00510
R6	Resistor, 4.02K, 1/4W, 1%	617-00010
R7	Same as R6	
R8	Resistor, 1.1K, 1.4W, 1%	617-00023
R9	Resistor, 1K, 1/4W, 1%	617-00002
R10	Resistor, 4.22K, 1/2W, 1%,MF	618-00048
R11	Resistor, 10K, 1/4W, 1%	617-00012
R12	Resistor, 200Ω, 1W, 5%	597-00201
R13	Resistor, 3K, 1/4W, 5%	595-00302
R14	Resistor, 1.65K, 1/2W, 1%, MF	618-00011
R15	Resistor, 20Ω, 1/4W, 5%	595-00200
R16	Resistor, 1K, 1/4W, 1%	617-00002
R17	Resistor, 620Ω,1/2W, 5%	596-00621
R18	Resistor, 47Ω, 1/2W, 5%	596-00470
R19	Resistor, 15.4K, 1/2W, 1%, MF	618-00072
R20	Resistor, 1K, 1/4W, 1%	617-00002
R21	Resistor, 1K, 1/4W, 1%	617-00002
R22	Resistor, 15K, 1/2W, 1%, MF	618-00092
R23	Trimpot, 1K	551-00040
R24	Resistor, 100Ω,1/4W, 5%	595-00101
R25	Resistor, 71.5K, 1/4W, 1%	617-00031
R26	Resistor, 100Ω, 1/4W, 5%	595-00101
R27	Resistor, 10K, 1/4W, 1%	617-00012
R28	Resistor, 100K, 1/4W, 1%	617-00016
R29	Resistor, 4.99K, 1/4W, 1%	617-00011
R30	Resistor, 100K, 1/4W, 1%	617-00016
R31	Resistor, 2K, 1/4W, 5%	595-00202
R32	Resistor, 316Ω, 1/4W, 1%	617-00027
R33	Resistor, 470Ω, 1/2W, 5%	596-00471
R34	Resistor, 475Ω, 1/4W, 1%	617-00026
R35	Resistor, 1.8K, 1/4W, 1%	617-00021
R36	Trimpot, 200Ω	551-00039
R37	Resistor, 200K, 1/4W, 1%	617-00017
R38	Trimpot, 10K	551-00033
R39	Resistor, 750K, 1/2W, 1%, MF	618-00091
R40	Resistor, 51Ω, 1/4W, 5%	595-00510
R41	Resistor, 51Ω, 1/4W, 5%	595-00510
R42	Same as R41	
R43	Resistor, 300Ω, 3W, ww	610-00061
R44	Same as R40	
R45	Resistor, 1.5K, 1/4W, 5%	595-00152
R46	Resistor, 330Ω, 1/2W, 5%	596-00331
R47	Same as R26	
R48	Same as R44	
R49	Same as R46	
R50	Same as R41	
R51	Resistor, 470Ω, 1W, 5%	597-00471
R52	Resistor, 10Ω, 1/2W, 5%	596-00100
R53	Resistor, 200Ω, 1/2W, 5%	596-00100
R54	Resistor, 200Ω, 1W, 5%	597-00201

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
T1	Transformer	651-12686
T2	Transformer	651-12687

5-4 STRETCHER BOARD

C1	Cap., .01μF; cer	311-00012
C2	Cap., 2500 pF; poly	326-00011
C3	Cap., 75 pF; cer.	311-00025
C4	Cap., 50 pF; cer.	311-00006
C5	Cap., 100 pF; cer.	311-00007
C6	Cap., 20 pF; cer;	311-00002
C7	Cap., 240 pF; poly	311-00021
C8	Cap., 25 pF; cer.	311-00003
C9	Cap., .001 μF; cer.	311-00010
C10	Cap., Same as C8	
C11	Cap., Same as C6	
C12	Cap., Same as C4	
C13	Cap., 200 pF; poly.	326-00016
C14	Cap., Same as C6	
C15	Cap., 30 pF; cer.	311-00005
C16	Cap., 300 pF. poly	326-00022
C17	Cap., 25 μF; 25V Elector	316-00028
C18	Cap., 0.1 μF cer.	311-00034
C19	Cap., same as C17	
C20	Cap., same as C18	
C21	Cap., Same as C18	
C22	Cap., Same as C6	
CR1	Diode, 1N756	374-00064
CR1A	Diode, Spec M Quad	376-11760
CR1B	Diode, Same as CR1A	
CR1C	Diode, Same as CR1A	
CR1D	Diode, Same as CR1A	
CR2	Diode	376-11764
CR3	Diode 1N756	374-00064
CR4	Diode	374-12529
CR5	Diode	376-11764
CR6A	Diode	374-11761
CR6B	Diode, Same as CR6A	
CR7	Diode, Same as CR2	
CR8	Diode, Same as CR2	
Q1A	Transistor	663-00092
Q1B	Transistor, Same as Q1B	
Q2	Transistor,	663-11749
Q3A	Transistor	663-11759
Q3B	Transistor, Same as Q3A	
Q4	Transistor, Same as Q2	
Q5	Transistor	663-11724
Q6	Transistor	663-00070
Q7	Transistor, Same as Q6	
Q8	Transistor	663-00071
Q9	Transistor, Same as Q5	
Q10	Transistor, Same as Q6	
Q11	Transistor, Same as Q6	
Q12	Transistor	663-11757
Q13	Transistor, Same as Q12	

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
Q14	Transistor, Same as Q12	
Q15	Transistor, Same as Q12	
Q16	Transistor, Same as Q2	
Q17	Transistor, Same as Q12	
Q18	Transistor, Same as Q12	
Q19	Transistor, Same as Q12	
Q20	Transistor, Same as Q12	
R1	Resistor, 15.4K, 1/2W, 1%	618-00072
R2	Resistor, Same as R1	
R3	Resistor, 22M, 1/4W, 5%	595-00226
R4	Resistor, Same as R3	
R5	Resistor, Same as R3	
R6	Resistor, Same as R3	
R7	Resistor, Same as R3	
R8	Resistor, 40.2K, 1/2W, 1%	618-00064
R9	Resistor, Same as R8	
R10	Resistor, 1K, 1/4W, 5%	595-00102
R11	Resistor, 10K, 1/4W, 1%	617-00012
R12	Resistor, 2K, 1/4W, 5%	595-00202
R13	Resistor, 7.5K, 1/4W, 5%	595-00752
R14	Resistor, 2.7K, 1/4W, 5%	595-00272
R15	Resistor, 3K, 1/4W, 5%	595-00302
R16	Resistor, 100Ω, 1/4W, 5%	595-00101
R17	Resistor, 2.4K, 1W, 5%	597-00242
R18	Resistor, 2K, 1/4W, 1%	617-00003
R19	Resistor, 866Ω, 1/2W, 1%	618-00067
R20	Trim pot, 200Ω,	551-00039
R21	Resistor, 402K, 1/2W, 1%	617-00018
R22	Trim pot, 20K	551-00034
R23	Resistor, 1K, 1/4W, 1%	617-00002
R24	Not used	
R25	Not used	
R26	Resistor, 1Meg, 1/4W, 5%	595-00105
R27	Resistor, 12K, 1/4W, 5%	595-00123
R28	Resistor, Same as R10	
R29	Resistor, Same as R27	
R30	Resistor, Same as R16	
R31	Resistor, 10K, 1/4W, 5%	595-00103
R32	Resistor, 2K, 1W, 5%	597-00202
R33	Resistor, 10K, 1/2W, 1/4%	614-00003
R34	Resistor, 1.11K, 1/2W, 1/4%	614-00001
R35	Resistor, 1K, 1/2W, 1%	618-00007
R36	Resistor, 511K, 1/2W, 1%	618-00013
R37	Not used	
R38	Resistor, Same as R12	
R39	Resistor, 300Ω, 1/2W, 5%	596-00301
R40	Resistor, 75Ω, 1/4W, 5%	595-00750
R41	Resistor, 680Ω, 1/4W, 5%	595-00681
R42	Resistor, 910Ω, 1/2W, 5%	596-00911
R43	Resistor, Same as R40	
R44	Resistor, Same as R41	
R45	Resistor, 1.5K, 1/4W. 5%	595-00152
R46	Resistor, 150K, 1/4W, 5%	595-00154
R47	Resistor, 6.8Ω, 1/4W, 5%	595-00682
R48	Resistor, Same as R10	
R49	Resistor, Same as R31	
R50	Resistor, Same as R45	
R51	Trim pot, 10K	551-00033
R52	Resistor, Same as R15	
R53	Resistor, 330Ω, 1/2W, 5%	596-00331
R54	Resistor, 200Ω, 1/4W, 5%	595-00201
R55	Resistor, Same as R15	
R56	Resistor, Same as R42	
R57	Resistor, Same as R16	
R58	Resistor, Same as R54	
R59	Resistor, 10Ω, 1/2W, 5%	596-00100
R60	Resistor, 47Ω, 1/4W, 5%	595-00470
R61	Resistor, Same as R15	
R62	Resistor, 120Ω, 1/4W, 5%	
R63	Resistor, Same as R10	
R64	Resistor, 750Ω, 1/4W, 5%	595-00751
R65	Resistor, 30K, 1/4W, 5%	595-00303
R66	Resistor, Same as R45	
R67	Resistor, Same as R64	
R68	Resistor, Same as R45	
R69	Resistor, Same as R47	
R70	Resistor, Same as R46	
R71	Resistor, Same as R31	
R72	Resistor, Same as R65	
R73	Resistor, Same as R45	
R74	Resistor, Same as R64	
R75	Resistor, Same as R64	
R76	Resistor, Same as R45	
R77	Resistor, 3.3K, 1/4W, 5%	595-00332
R78	Resistor, Same as R47	
R79	Resistor, Same as R46	
R80	Resistor, 15K, 1/4W, 5%	595-00153
R81	Resistor, Same as R45	
R82	Resistor, Same as R59	
R83	Resistor, Same as R59	

5-5 TRIGGER BOARD

C1	Cap., 1μF, 50V	311-00034
C2	Cap., 1μF, 50V	311-00034
C3	Cap., 1μF, Mylar	320-00011
C4	Cap., 25pF, Disc.	311-00003
C6	Cap., 410pF	311-00071
C7	Cap., .001μF	311-00010
C8	Cap., .01μF	311-00012
C9	Cap., 1000pF, Poly	311-00005
C10	Cap., 423pF, 1%	311-00070
C11	Cap., 047μF, 1%	320-00040
C12	Cap., .47μF, 1%	320-00041
C13	Cap., .25μF, 25V	316-00028
C14	Cap., .1μF, 50V	311-00034
C15	Cap., Same as C13	
C16	Cap., Same as C1	
C17	Cap., 15μF, 50V	316-00062
C18	Cap., Same as C8	
C19	Cap., 7-15pF	332-00005

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
C20	Cap., Same as C7	
C21	Cap., 2.2μF, 25V	311-00019
CR1	Diode, 1N3719TD	376-00053
CR2	Diode, zener	374-12529
CR3	Diode	376-11764
CR4	Diode, Same as CR1	
CR5	Diode, zener	374-00019
CR6	Diode,, same as CR2	
CR7	Diode, Same as CR3	
CR8A	Diode, zener	374-11761
CR8B	Diode, zener, Same as CR8A	
CR9	Diode, zener, 1N756A	374-00064
CR10	Diode	376-11742
CR11	Diode, Same as CR10	
CR12	Diode, zener, same as CR6	
CR13	Diode, Same as CR10	
CR14	Diode, Same as CR7	
CR15A	Diode, Zener	374-11730
CR15B	Diode, zener, Same as CR15A	
CR16	Diode, Same as CR7	
CR17	Diode, Same as CR7	
CR18	Diode, Same as CR7	
CR19	Diode, Zener, Same as CR6	
CR20	Diode, Same as CR7	
CR21	Diode, Same as CR7	
CR22	Diode, Same as CR7	
L1	Choke, .68μH	335-00013
L2	Choke, Same as L1	
Q1	Transistor, MP 11749	663-12973
Q2	Transistor, Same as Q1	
Q3	Transistor	663-11749
Q4	Transistor	663-11477
Q5	Transistor, Same as Q4	
Q6	Transistor	663-11757
Q7	Transistor, Same as Q6	
Q8	Transistor, Same as Q3	
Q9	Transistor, Same as Q3	
Q10	Transistor, Same as Q3	
Q11	Transistor, Same as Q3	
Q12	Transitor, Same as Q6	
Q13	Transistor, Same as Q6	
Q14	Transitor, MM709	663-00093
Q15	Transistor, 1N3251	663-00076
Q16	Transistor,	663-11762
Q17	Transistor, Same as Q16	
Q18	Transistor, Same as Q16	
Q19	Transistor, Same as Q6	
Q20	Transistor, Same as Q6	
Q21	Transistor, Same as Q3	
Q22	Transistor, Same as Q3	
Q23	Transistor, Same as Q6	
Q24	Transistor, Same as Q6	
Q25	Transistor, Same as Q6	

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
Q26	Transistor, Same as Q6	
Q27	Transistor, Same as Q15	
Q28	Transistor, 2N3904	663-00070
R1	Resistor, 51Ω, 1/2W, 5%	596-00511
R2	Resistor, 100Ω, 1/4W, 5%	595-00101
R3	Resistor, 1.21K, 1/2W, 1%	618-00023
R4	Resistor, 20Ω, 1/4W, 5%	595-00200
R5	Resistor, 560Ω, 1/4W, 5%	595-00561
R6	Resistor, 100Ω, 1/4W, 5%	595-00101
R7	Resistor, 390Ω, 1/4W, 5%	595-00391
R8	Resistor, Same as R4	
R9	Resistor, 5.1Ω, 1/4W, 5%	595-00051
R10	Resistor, 470Ω, 1/2W, 5%	596-00471
R11	Resistor, Same as R2	
R12	Resistor, 2K, 1/4W, 5%	595-00202
R13	Resistor, 1.8K, 1/2W, 5%	596-00182
R14	Resistor, 15Ω, 1/4W, 5%	595-00150
R15	Resistor, 1K, 1/4W, 5%	595-00102
R16	Resistor, Same as R2	
R17	Resistor, 249Ω, 1/2W, 1%	618-00016
R18	Resistor, 1.5K, 1/4W, 5%	595-00152
R19	Resistor, 2K, 1/4W, 5%	595-00202
R20	Resistor, 240Ω, 1/4W, 5%	595-00241
R21	Resistor, 680Ω, 1/2W, 5%	596-00681
R22	Resistor, 10Ω, 1/4W, 5%	595-00100
R23	Resistor, 1.21K, 1/2W, 1%	618-00023
R24	Resistor, 18Ω, 1/4W, 5%	595-00180
R25	Resistor, Same as R4	
R26	Resistor, 1K, 1/2W, 1%	618-00007
R27	Resistor, 620Ω, 1/4W, 5%	595-00621
R28	Resistor, 100Ω, 1/4W, 5%	595-00101
R29	Resistor, Same as R18	
R30	Resistor, Same as R2	
R31	Resistor, 620Ω, 1/4W, 5%	595-00621
R32	Resistor, 360Ω, 1/2W, 5%	596-00361
R33	Resistor, 200Ω, 1/4W, 5%	595-00201
R34	Resistor, Same as R2	
R35	Resistor, Same as R18	
R36	Resistor, 33K, 1/4W, 5%	595-00333
R37	Resistor, 10Ω, 1/4W, 5%	595-00100
R38	Resistor, 3.6K, 1/2W, 5%	596-00362
R39	Resistor, Same as R2	
R40	Resistor, 820Ω, 1/2W, 5%	596-00821
R41	Resistor, Same as R2	
R42	Resistor, 432Ω, 1/2W, 1%	618-00093
R43	Resistor, 100Ω, 1/2W, 1%	618-00025
R44	Resistor, 10Ω, 1/4W, 5%	595-00100
R45	Resistor, 470Ω, 1/2W, 5%	596-00471
R46	Resistor, 200Ω, 1/4W, 5%	595-00201
R47	Resistor, Same as R12	
R48	Resistor, 3K, 1/4W, 5%	595-00302
R49	Resistor, Same as R15	
R50	Trim pot, 2K	551-00038
R51	Resistor, 560Ω, 1/4W, 5%	595-00561
R52	Resistor, Same as R18	

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
R53	Resistor, 330Ω, 1/2W, 5%	596-00331
R54	Resistor, Same as R18	
R55	Resistor, 270Ω, 1/4W, 5%	595-00271
R56	Resistor, Same as R15	
R57	Resistor, Same as R2	
R58	Resistor, Same as R18	
R59	Resistor, Same as R2	
R60	Resistor, 750Ω, 1/2W, 5%	596-00751
R61	Resistor, Same as R60	
R62	Resistor, Same as R60	
R63	Resistor, 51Ω, 1/4W, 5%	595-00510
R64	Resistor, Same as R63	
R 65	Helitrim 500Ω	551-00044
R66	Resistor, Same as R2	
R67	Resistor, 15Ω, 1/4W, 5%	595-00150

5-6 COUNTER BOARD

CR1	Diode	376-11742
CR2	Diode, Same as CR1	
CR3	Diode, Same as CR1	
CR4	Diode, Same as CR1	
CR5	Diode, Same as CR1	
CR6	Diode, Same as CR1	
CR7	Diode, Same as CR1	
CR8	Diode, Same as CR1	
CR9	Diode, Same as CR1	
CR10	Diode, Same as CR1	
CR11	Diode, Same as CR1	
CR12	Diode, Same as CR1	
IC1	Int. Ckt. 832P	665-00009
IC2	Same as IC1	
IC3	Int. Ckt. 815P	665-00007
IC4	Same as IC3	
IC5	Int. Ckt. 817P	665-00008
IC6	Same as IC1	
IC7	Same as IC3	
IC8	Same as IC5	
IC9	Same as IC1	
IC10	Int. Ckt. 890P	665-00010
IC11	Int. Ckt. 890P	665-00010
IC12	Same as IC10	
IC13	Same as IC10	
IC14	Same as IC10	
IC15	Same as IC10	
Q1	Transistor, 1N3904	663-00070
Q2	Transistor, Same as Q1	
Q3	Transistor, Same as Q1	
Q4	Transistor, Same as Q1	
Q5	Transistor, Same as Q1	
Q6	Transistor, Same as Q1	
Q7	Transistor, Same as Q1	
Q8	Transistor, Same as Q1	
Q9	Transistor, Same as Q1	
Q10	Transitor, Same as Q1	
Q11	Transistor, Same as Q1	
Q12	Transistor, Same as Q1	
R1	Resistor, 360Ω, 1/4W, 5%	595-00361
R2	Resistor, 1.5K, 1/4W, 5%	595-00152
R3	Resistor, Same as R1	
R4	Resistor, Same as R2	
R5	Resistor, Same as R1	
R6	Resistor, Same as R2	
R7	Resistor, Same as R1	
R8	Resistor, Same as R2	
R9	Resistor, Same as R1	
R10	Resistor, Same as R2	
R11	Resistor, Same as R1	
R12	Resistor, Same as R2	
R13	Resistor, Same as R1	
R14	Resistor, Same as R2	
R15	Resistor, Same as R1	
R16	Resistor, Same as R2	
R17	Resistor, Same as R1	
R18	Resistor, Same as R2	
R19	Resistor, Same as R1	
R20	Resistor, Same as R2	
R21	Resistor, Same as R1	
R22	Resistor, Same as R2	
R23	Resistor, Same as R1	
R24	Resistor, Same as R2	

5-7 BUFFER BOARD

C1	Cap., .005μF, 1kv	311-00011
C2	Cap., 0.1μF, 50 V	311-00034
C3	Cap., 250pF cer.	311-00004
CR1	Diode, zener, 1N753	374-00058
CR2	Diode, 1N914B	376-00022
CR3	Diode	376-11742
Q1A,1B	Transistor Dual mpn	663-20000
Q1	Transistor, 2N3904	663-00070
Q2	Transistor, Same as Q1	
Q3	Transistor, 2N3251	663-00076
Q4	Transistor, Same as Q3	
Q5	Transistor, Same as Q1	
Q6	Transistor, 2N3906	663-00071
Q7	Transistor, Same as Q1	
Q8	Transistor, Same as Q6	
Q9	Transistor, Same as Q1	
Q10	Transistor, Same as Q6	
R1	Resistor, 1.87K, 1/2W, 1%	618-00017
R2	Trimpot, 200Ω	551-00039
R3	Resistor, 12K, 1/4W, 5%	595-00123
R4	Resistor, 49.9Ω, 1/2W, 1%	618-00090
R5	Resistor, 1K, 1/4W, 5%	595-00102

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
R6	Resistor, 536Ω, 1/2W, 1%	618-00074
R7	Resistor, 30K, 1/4W, 5%	595-00303
R8	Resistor, Same as R3	
R9	Resistor, Same as R5	
R10	Resistor, 2K, 1/2W, 1%	618-00005
R11	Resistor, Same as R10	
R12	Resistor, 249K, 1/2W, 1%	618-00068
R13	Trimpot, 20K	551-00034
R14	Resistor, 3.9K, 1/2W, 5%	596-00392
R15	Resistor, 1K, 1/2W, 1%	618-00007
R16	Trimpot, Same as R2	
R17	Resistor, 374Ω, 1/2W, 1%	618-00028
R18	Resistor, 100Ω, 1/4W, 5%	595-00101
R19	Resistor, Same as R5	
R20	Trimpot, 2K	551-00038
R21	Resistor, 1.8K, 1/4W, 5%	595-00182
R22	Resistor, 390Ω, 1/4W, 5%	595-00391
R23	Resistor, 3.6K, 1/4W, 5%	595-00362
R24	Resistor, 4.3K, 1/4W, 5%	595-00432
R25	Resistor, 150K, 1/4W, 5%	595-00154
R26	Resistor, 10K, 1/4W, 5%	595-00103
R27	Resistor, Same as R22	
R28	Resistor, Same as R23	
R29	Resistor, Same as R24	
R30	Resistor, Same as R25	
R31	Resistor, Same as R26	
R32	Resistor, Same as R22	
R33	Resistor, Same as R23	
R34	Resistor, Same as R24	
R35	Resistor, Same as R25	
R36	Resistor, Same as R26	

5-8 POWER SUPPLY REGULATOR

C1	Cap., 25μF, 25V	316-00028
C2	Cap., 100μF, 25V	316-00035
C3	Cap., 0.1μF, 50V	311-00034
C4	Same as C1	
C5	Same as C2	
C6	Same as C1	
C7	Cap, Same as C2	
C8	Cap., Same as C3	
C9	Cap. Same as C1	
C10	Cap. Same as C2	
C11	Cap., 100μF, 6V	316-00068
CR1	Diode, 1N914B	376-00022
CR2	Diode, Same as CR1	
CR3	Diode, 1N4005	376-00034
CR4	Diode, Same as CR1	
CR5	Diode, zener, 1N936A	374-00068
CR6	Diode, Zener, 1N749A	374-00044
Q1	Transistor	663-11724
Q2	Transistor, Same as Q1	
Q3	Transistor	663-11725
Q4	Transistor, Same as Q3	
Q5	Transistor, Same as Q3	
Q6	Transistor, Same as Q1	
Q7	Transistor, Same as Q1	
Q8	Transistor, Same as Q1	
Q9	Transistor, Same as Q3	
Q10	Transistor, Same as Q3	
Q11	Transistor, Same as Q3	
Q12	Transistor, Same as Q3	
Q13	Transistor, Same as Q1	
R1	Resistor, 1K, 1/2W, 5%	596-00102
R2	Resistor, 100Ω, 1/2W, 5%	596-00101
R3	Resistor, 5.1K, 1/2W, 5%	596-00512
R4	Resistor, 1.8K, 1/2W, 5%	596-00182
R5	Resistor, 680Ω, 1/2W, 5%	596-00681
R6	Potentiometer, 200Ω	551-00039
R7	Resistor, 1.3K, 1/2W, 5%	596-00132
R8	Resistor, 1K, 1/2W, 5%	596-00102
R9	Resistor, 470Ω, 1/2W, 5%	596-00471
R10	Resistor, 820Ω, 1/2W, 5%	596-00821
R11	Resistor, 5.6K, 1/2W, 5%	596-00562
R12	Resistor, 5.6K, 1/2W, 1%	618-00045
R13	Resistor, Same as R12	
R14	Resistor, 33K, 1/2W, 5%	596-00333
R15	Resistor, Same as R5	
R16	Resistor, Same as R8	
R17	Resistor, 200Ω, 1/2W, 5%	596-00201
R18	Resistor, Same as R7	
R19	Resistor, 750Ω, 1/2W, 5%	596-00751
R20	Potentiometer, Same as R6	
R21	Resistor, Same as R9	
R22	Resistor, 2.7K, 1/2W, 5%	596-00272
R23	Resistor, 1.5K, 1/2W, 5%	596-00152
R24	Resistor, 3K, 1/2W, 5%	596-00302
R25	Resistor, 120Ω, 1/2W, 5%	596-00121
R26	Resistor, Same as R23	
R27	Resistor, 1K, 1/2W, 1%	618-00007
R28	Resistor, Same as R27	
R29	Resistor, 510Ω, 1/2W, 1%	596-00511
R30	Resistor, 750Ω, 1/2W, 5%	596-00757
R31	Resistor, 62Ω, 1/2W, 5%	596-00620
R32	Resistor, 2K, 1/2W, 5%	596-00202

5-9 D/A CONVERTER BOARD

C4	Cap., 25μF, 25V, Elec	316-00028
C5	Cap., .001μF, Cer.	311-00010
CR2	Diode, zener, 1N753	374-00019
Q4	Transistor, 2N1132	663-00024
Q5	Transistor, 2N3906	663-00071
Q6	Transistor, 2N3904	663-00070
Q7	Transistor, Same as Q6	
Q8	Transistor, Same as Q5	
Q9	Transistor, Same as Q6	
Q10	Transistor, Same as Q6	

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
Q11	Transistor, Same as Q5	
Q12	Transistor, Same as Q6	
Q13	Transistor, Same as Q6	
Q14	Transistor, Same as Q5	
Q15	Transistor, Same as Q6	
Q16	Transistor, Same as Q6	
Q17	Transistor, Same as Q5	
Q18	Transistor, Same as Q6	
Q19	Transistor, Same as Q6	
Q20	Transistor, Same as Q5	
Q21	Transistor, Same as Q6	
Q22	Transistor, Same as Q6	
Q23	Transistor, Same as Q5	
Q24	Transistor, Same as Q6	
Q25	Transistor, Same as Q6	
Q26	Transistor, Same as Q5	
Q27	Transistor, Same as Q6	
Q28	Transistor, Same as Q6	
Q29	Transistor, Same as Q5	
Q30	Transistor, Same as Q6	
Q31	Transistor, Same as Q6	
Q32	Transistor, Same as Q5	
Q33	Transistor, Same as Q6	
Q34	Transistor, Same as Q6	
Q35	Transistor, Same as Q5	
Q36	Transistor, Same as Q6	
Q37	Transistor, Same as Q6	
Q38	Transistor, Same as Q5	
Q39	Transistor, Same as Q6	
Q40	Transistor, Same as Q6	
R12	Potentiometer, 10K	551-00033
R13	Resistor, 3K, 1/4W, 5%	595-00302
R14	Resistor, 200Ω, 3W, ww	610-00042
R15	Pot. 50Ω	551-00032
R16	Resistor, 50Ω, 3W, ww	610-00068
R17	Resistor, 560Ω, 3W, ww	610-00007
R18	Resistor, 6.2K, 1/4W, 5%	595-00622
R19	Resistor, 150K, 1/4W, 5%	595-00154
R21	Resistor, 2K, 1/4W, 5%	595-00202
R22	Resistor, Same as R21	
R23	Resistor, Same as R13	
R25	Resistor, 100K, 1/4W, 5%	595-00104
R26	Resistor, 499Ω, 1/4W, 1%, MF	617-00005
R27	Resistor, 1K, 1/4W, 1%	617-00002
R28	Resistor, 2K, 1/4W, 1%	617-00003
R29	Resistor, 4.02K, 1/4W, 1%	617-00010
R30	Resistor, 4.99K, 1/4W, 1%	617-00011
R31	Resistor, 10K, 1/4W, 1%	617-00012
R32	Resistor, 20K, 1/4W, 1%	617-00013
R33	Resistor, 40.2K, 1/4W, 1%	617-00014
R34	Resistor, 49.9K, 1/4W, 1%	617-00015
R35	Resistor, 100K, 1/4W, 1%	617-00016
R36	Resistor, 200K, 1/4W, 1%	617-00017
R37	Resistor, 402K, 1/4W, 1%	617-00018
R38	Resistor, 6.2K, 1/4W, 5%	595-00622
R39	Resistor, 150K, 1/4W, 5%	595-00154
R40	Resistor, 2K, 1/4W, 5%	595-00202
R41	Resistor, 390Ω, 1/4W, 5%	595-00391
R42	Resistor, 3K, 1/4W, 5%	595-00302
R43	Resistor, Same as R25	
R44	Resistor, Same as R38	
R45	Resistor, Same as R19	
R46	Resistor, Same as R40	
R47	Resistor, Same as R41	
R48	Resistor, Same as R42	
R49	Resistor, Same as R25	
R50	Resistor, Same as R38	
R51	Resistor, Same as R19	
R52	Resistor, Same as R40	
R53	Resistor, Same as R41	
R54	Resistor, Same as R42	
R55	Resistor, Same as R25	
R56	Resistor, Same as R38	
R57	Resistor, Same as R19	
R58	Resistor, Same as R40	
R59	Resistor, Same as R41	
R60	Resistor, Same as R42	
R61	Resistor, Same as R25	
R62	Resistor, Same as R38	
R63	Resistor, Same as R19	
R64	Resistor, Same as R40	
R65	Resistor, Same as R41	
R66	Resistor, Same as R42	
R67	Resistor, Same as R25	
R68	Resistor, Same as R38	
R69	Resistor, Same as R19	
R70	Resistor, Same as R40	
R71	Resistor, Same as R41	
R72	Resistor, Same as R42	
R73	Resistor, Same as R25	
R74	Resistor, Same as R38	
R75	Resistor, Same as R19	
R76	Resistor, Same as R40	
R77	Resistor, Same as R41	
R78	Resistor, Same as R42	
R79	Resistor, Same as R25	
R80	Resistor, Same as R38	
R81	Resistor, Same as R19	
R82	Resistor, Same as R40	
R83	Resistor, Same as R41	
R84	Resistor, Same as R42	
R85	Resistor, Same as R25	
R86	Resistor, Same as R38	
R87	Resistor, Same as R19	
R88	Resistor, Same as R40	
R89	Resistor, Same as R41	
R90	Resistor, Same as R42	
R91	Resistor, Same as R25	
R92	Resistor, Same as R38	

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
R93	Resistor, Same as R19	
R94	Resistor, Same as R40	
R95	Resistor, Same as R41	
R96	Resistor, Same as R42	
R97	Resistor, Same as R25	
R98	Resistor, Same as R38	
R99	Resistor, Same as R19	
R100	Resistor, Same as R40	
R101	Resistor, Same as R41	
R102	Resistor, Same as R42	
R103	Resistor, Same as R25	

5-10 MISCELLANEOUS

C101	Cap., 1500μF, 50V	316-00045
C102	Cap., 1500μF, 50V	316-00045
C103	Cap., Same as C102	
C104	Cap., Same as C102	
C105	Cap., Same as C102	
C106	Cap., Same as C102	
C107	Cap., Same as C102	
CR101	Diode, 1N4005	376-00034
CR102	Diode, Same as CR101	
CR103	Diode, Same as CR101	
CR104	Diode, Same as CR101	
CR105	Diode, 1N4720	376-00062
CR106	Diode, Same as CR105	
CR107	Diode, Same as CR105	
CR108	Diode, Same as CR105	
CR109	Diode, Same as CR101	
CR110	Diode, Same as CR101	
CR111	Diode, Same as CR101	
CR112	Diode, Same as CR101	
Q101	Transistor, 2N3767	663-00085
Q102	Transistor, Same as Q101	
Q103	Transistor,	663-11705
Q104	Transistor, Same as Q103	
Q105	Transistor, Same as Q103	
R101	Resistor, 2.7Ω, 1/2W, 5%	595-00027
R102	Resistor, Same as R101	
R103	Resistor, 50Ω, 3W	610-00068
R104	Resistor, Same as R103	
R105	Resistor, 1Ω, 3W	610-00069
R106	Resistor, Same as R105	
R107	Resistor, 3Ω, 3W	610-00048
R108	Resistor, 10Ω, 5W	610-00099
R109	Resistor, 1Ω, 3W	610-00069
R110	Resistor, 100K, 1/2W, 5%	596-00104
R201	Resistor, 8.89K, 1/2W, 1/4%, MF614-00002	
R202	Resistor, 1.11K, 1/2W, 1/4%, MF614-00001	
R203	Helipot, 1K, 10T	540-00010
R204	Dual Potentiometer Bridged T	550-00037
R205	Resistor, 51Ω, 1/2W, 5%	596-00510
R206	Resistor, Same as R205	
R207	Resistor, 1K, 1/4W, 5%	595-00102
R301	Potentiometer, 10K, 2W	545-00006
S201	POWER (Toggle)	630-00006
S202	OUTPUT GAIN (rotary)	624-00011
S203	TRIGGER POLARITY (toggle)	630-00013
S204	DELAY RANGE (rotary)	624-00055
S205	DELAY MULTI. SOURCE (Rotary)	624-00004
T101	Power Transformer	650-10618
T201	Core, e+2A	361-00011

SECTION 6
DRAWINGS

6-1 GENERAL INFORMATION

This section of the manual contains drawings or photographs of the subassemblies and circuits in the E-H Model 153 Strobing Voltmeter. The assembly drawings or photographs contain the component circuit designators and show the location of the wiring terminals. On the schematics, physical subassembly boundaries are shown as well as functional element names. The theory of operation is located in Section 3 and the parts list is located in Section 5.

Figure 6-1 is an outline dimension drawing of the rack-mount configuration without end-frames. Figures 6-2 through 6-8 show the component location. Refer to the drawings and photographs to determine the location of any specific component.

6-2 SCHEMATIC DIAGRAMS

There are eight schematics and one block diagram following the component location drawings. Insofar as possible, the convention of signal-flow from left to right and current-flow from bottom to top are adhered to in the diagrams. Drawing number nine is a master schematic (not a wiring diagram) showing the interconnection of all subassemblies and controls.

Component symbology and nomenclature follow generally-accepted practices. Resistance is given in ohms. Capacitor values less than 1 are in picofarads unless otherwise labeled. Multi-deck rotary switches are shown schematically inline.

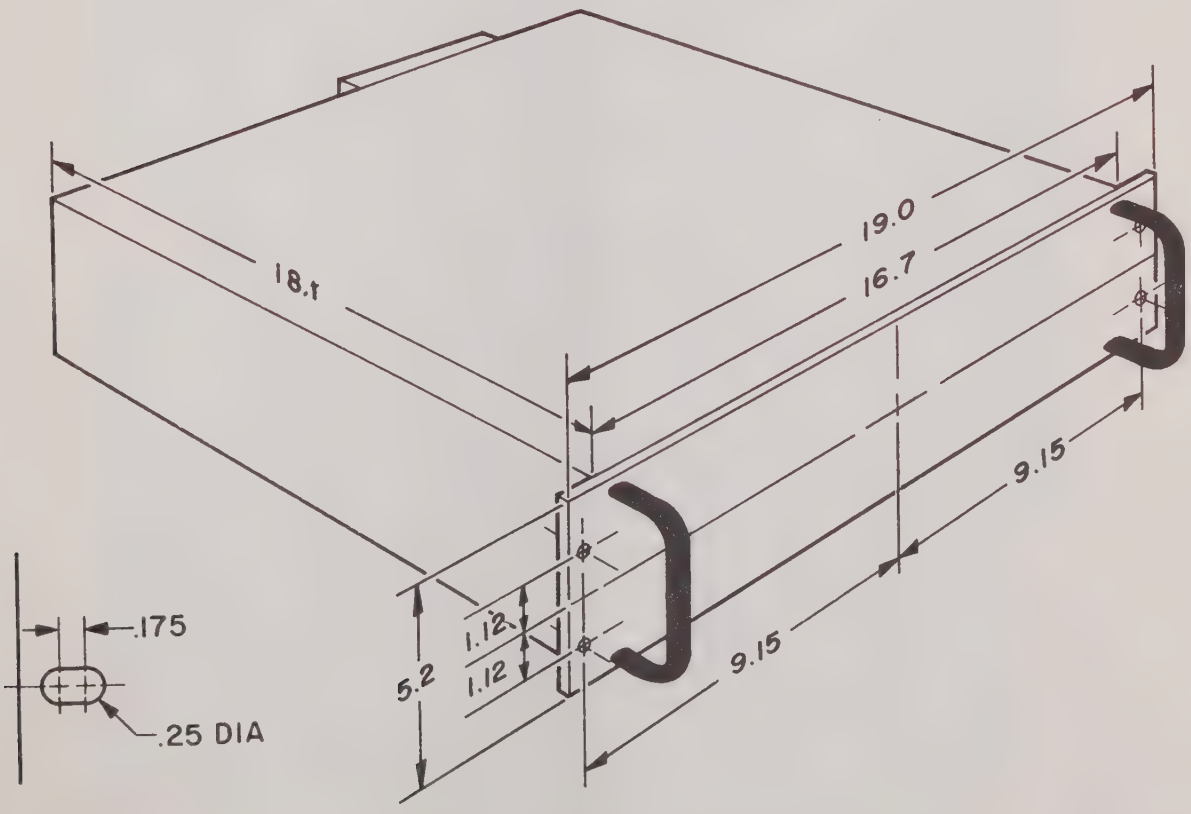


Figure 6-1 Outline Dimension Drawing

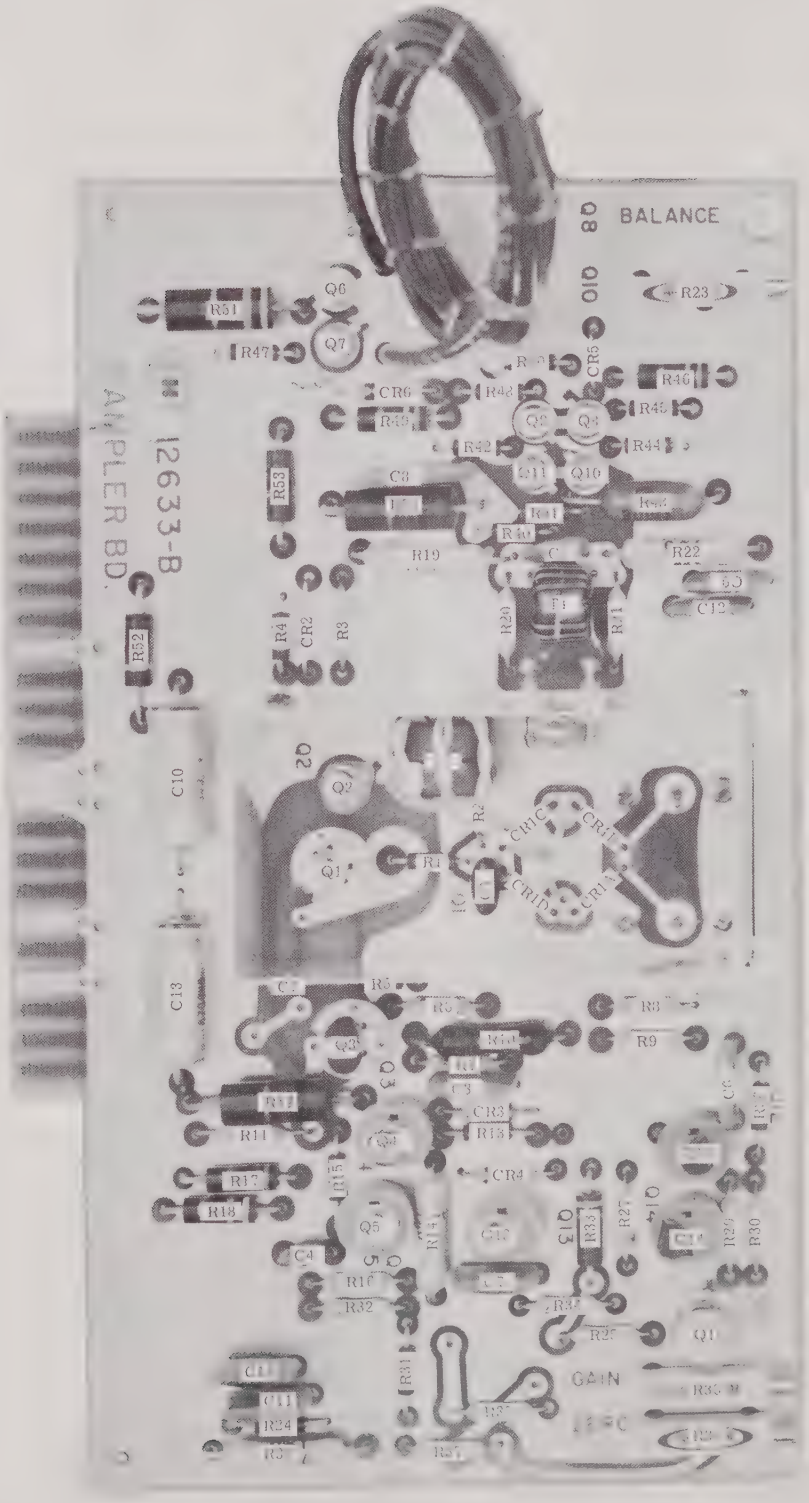


Fig. 6-2 Sampler Board 12634

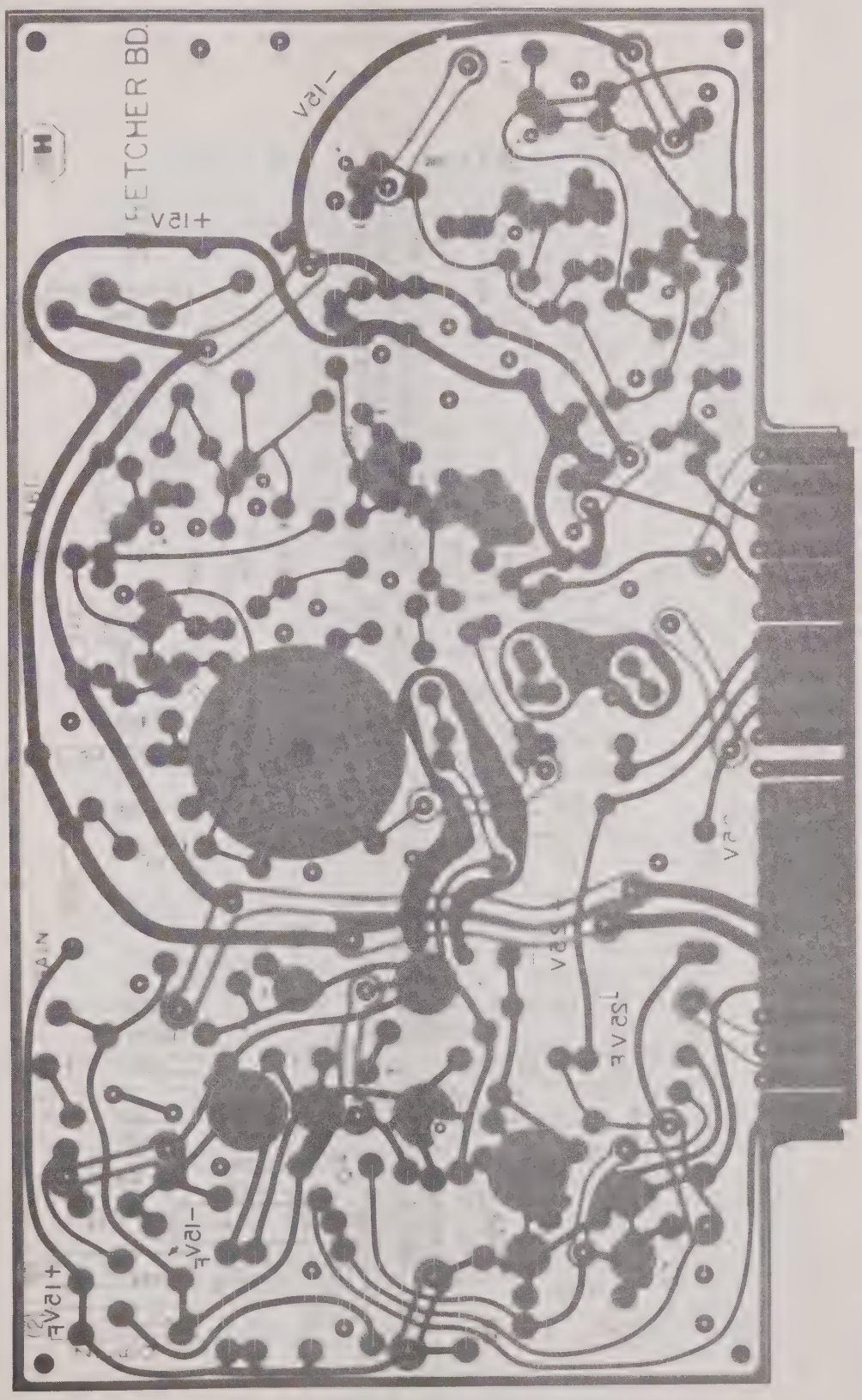


Figure 6-3 Stretcher Board 12637

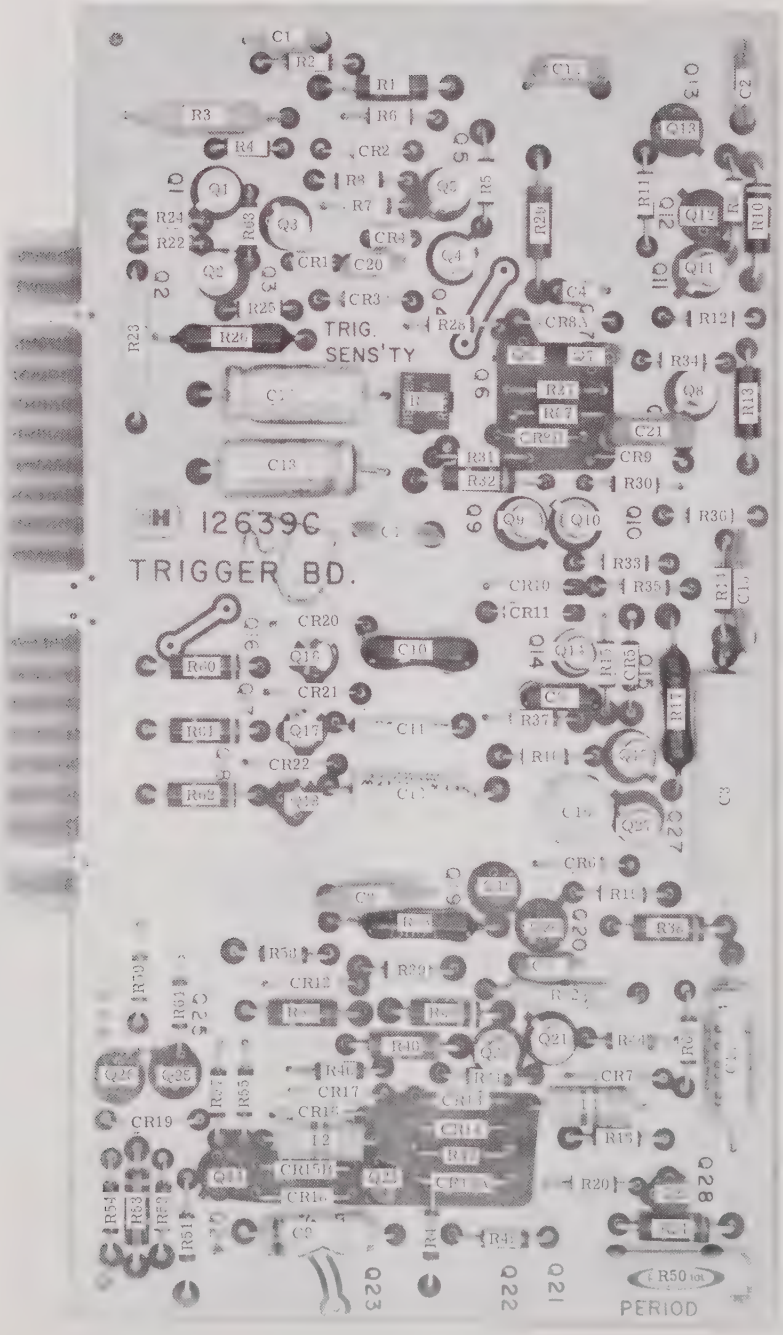


Fig. 6-4 Trigger Board 12640

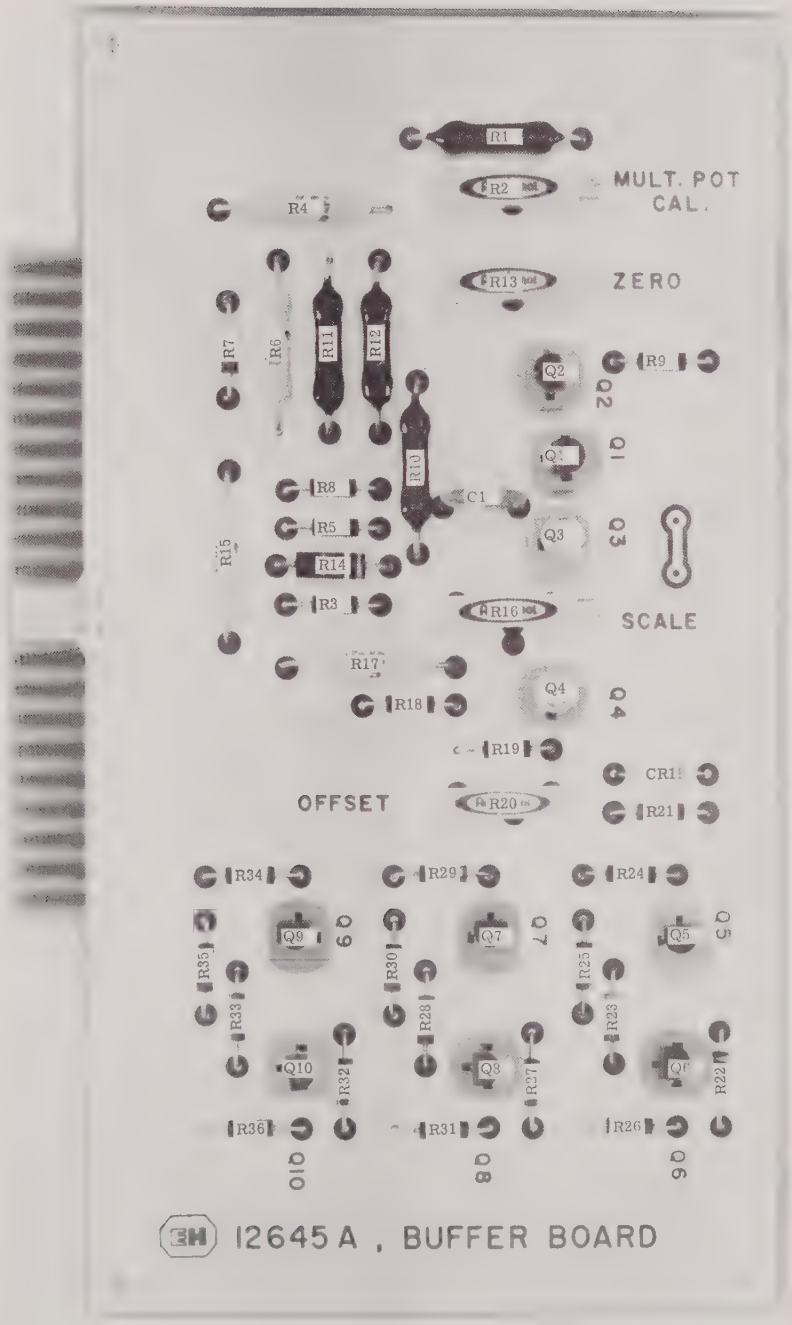


Fig. 6-5 Buffer Board 12646

Fig. 6-6 D/A Converter Board 12652

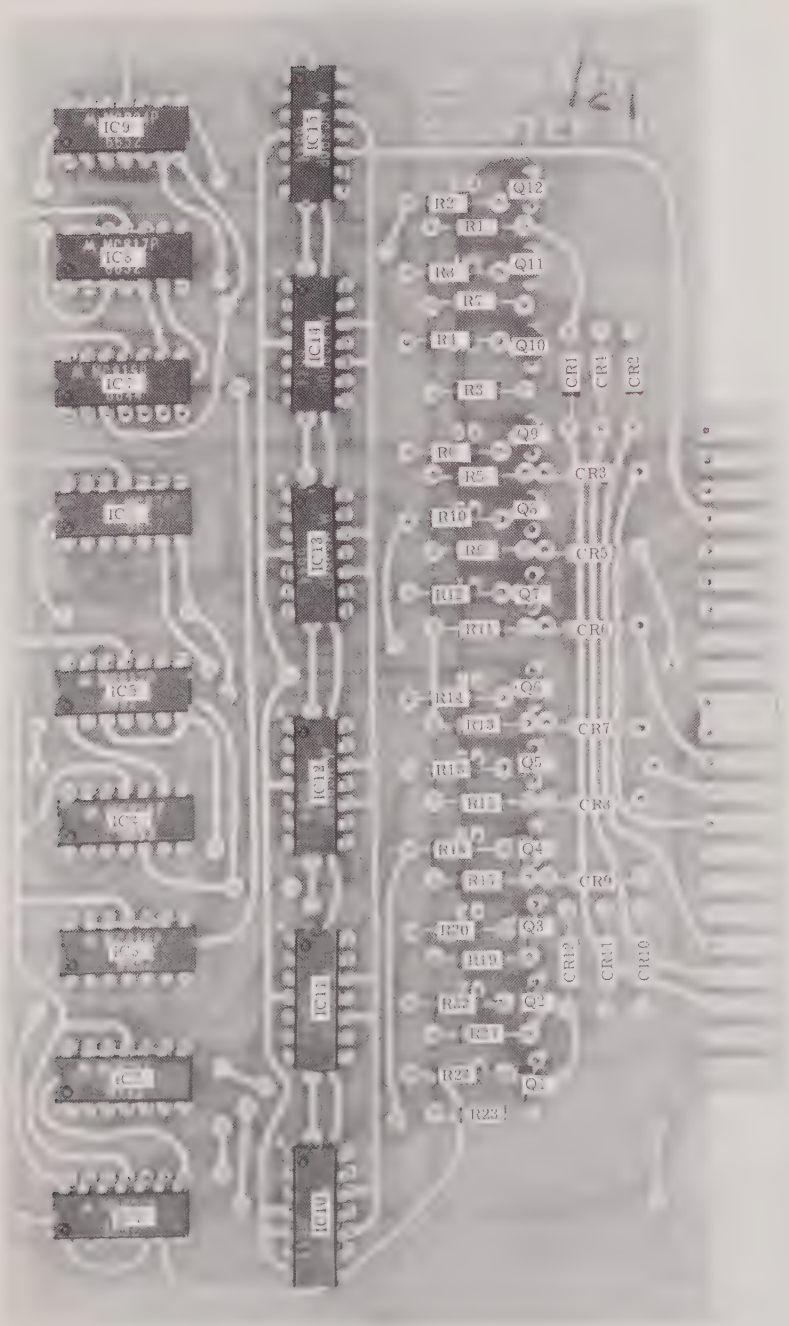


Fig. 6-7 Counter Board 12643

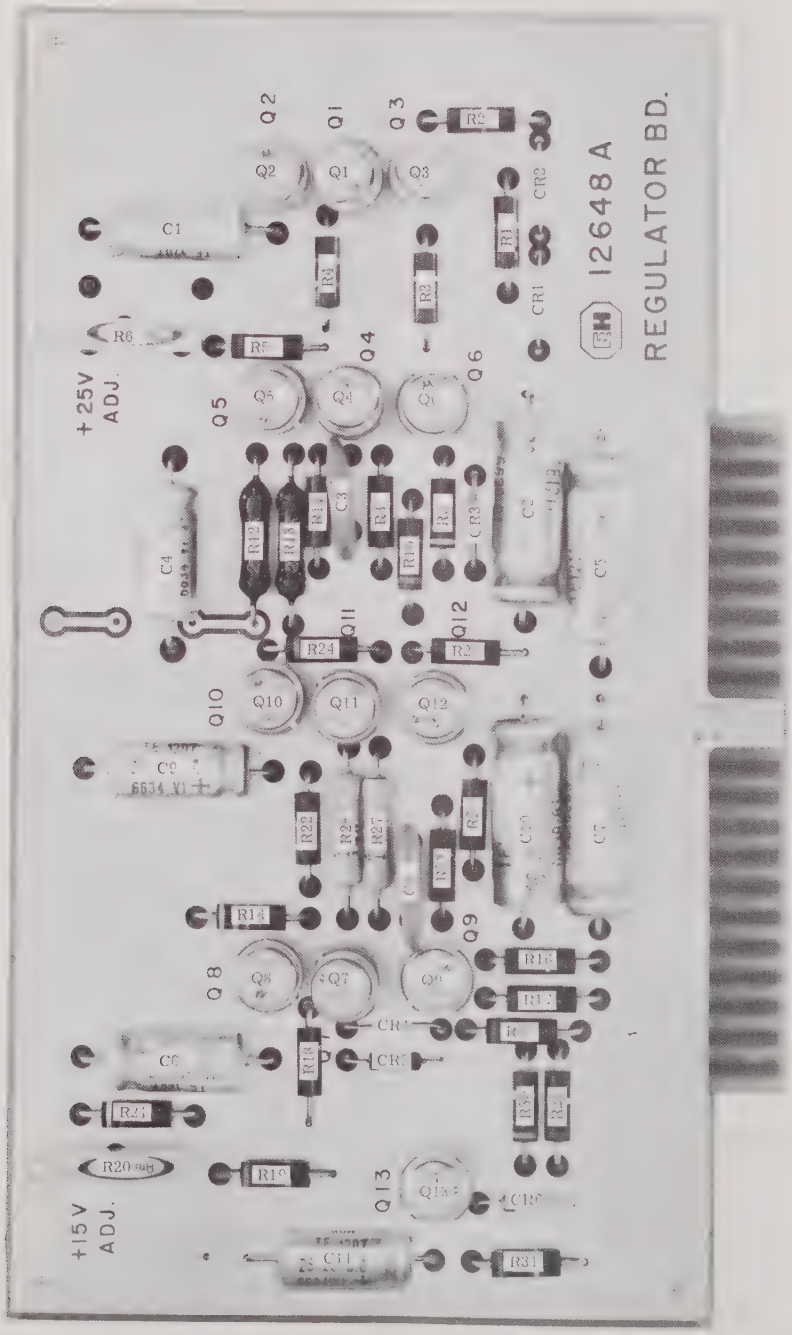


Fig. 6-8 Regulator Board 12649

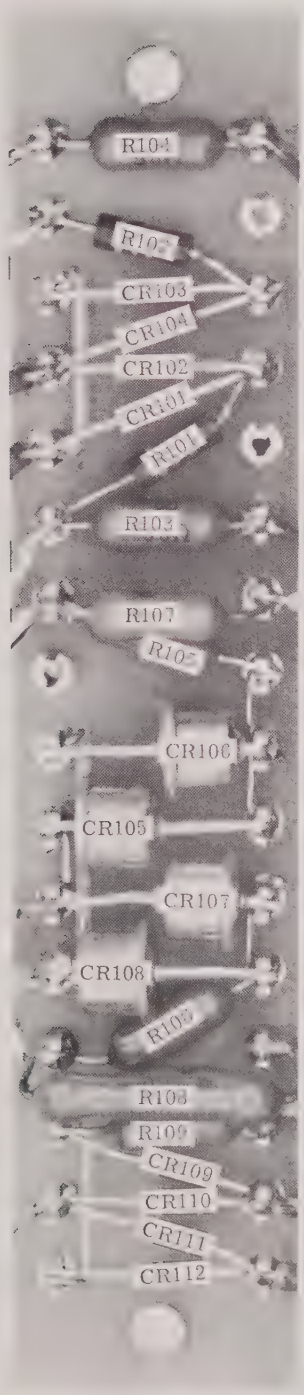
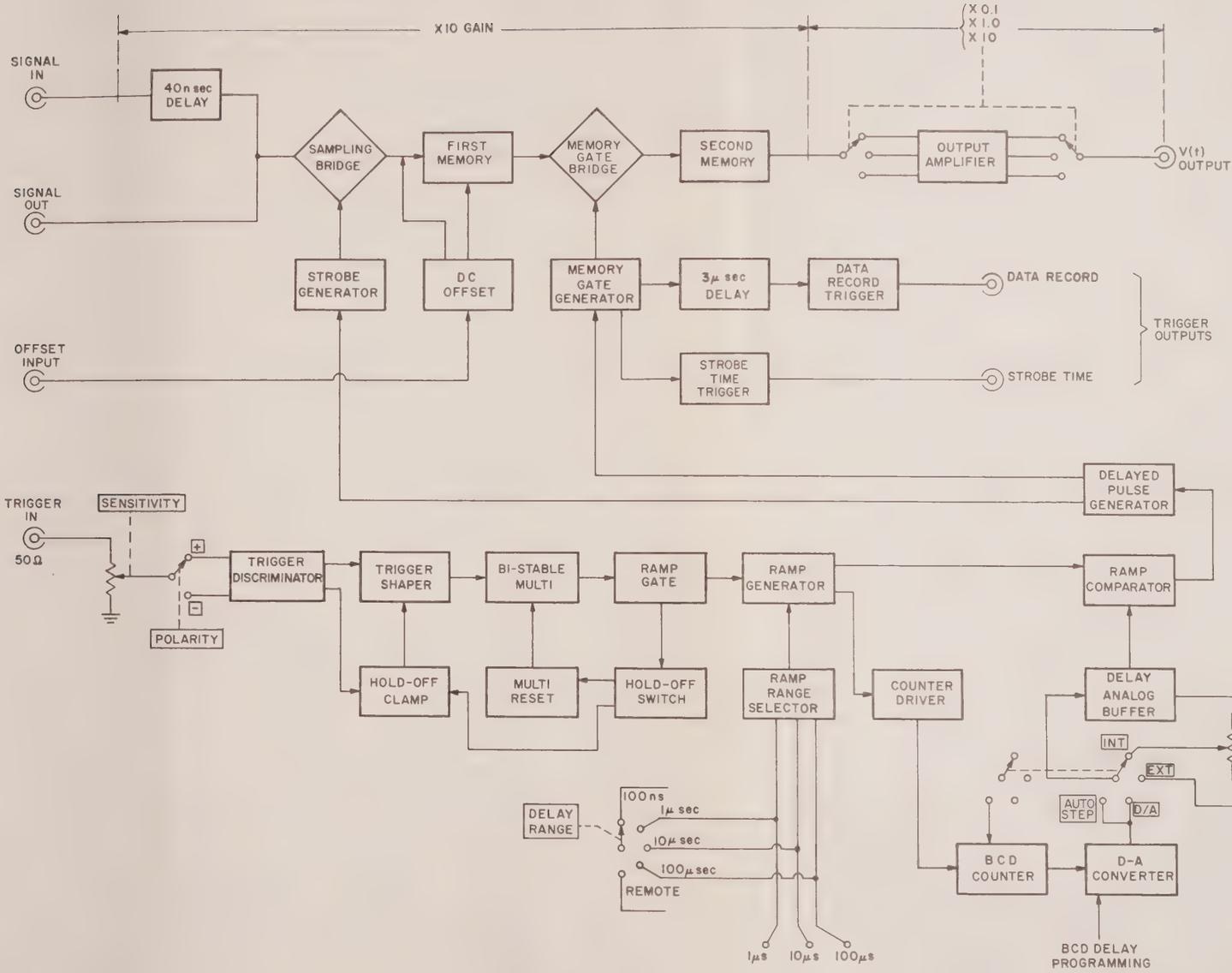
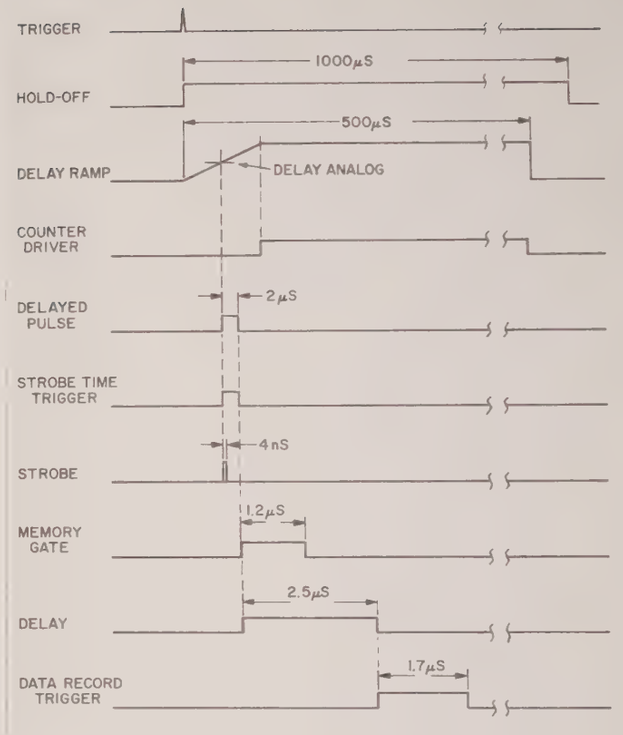
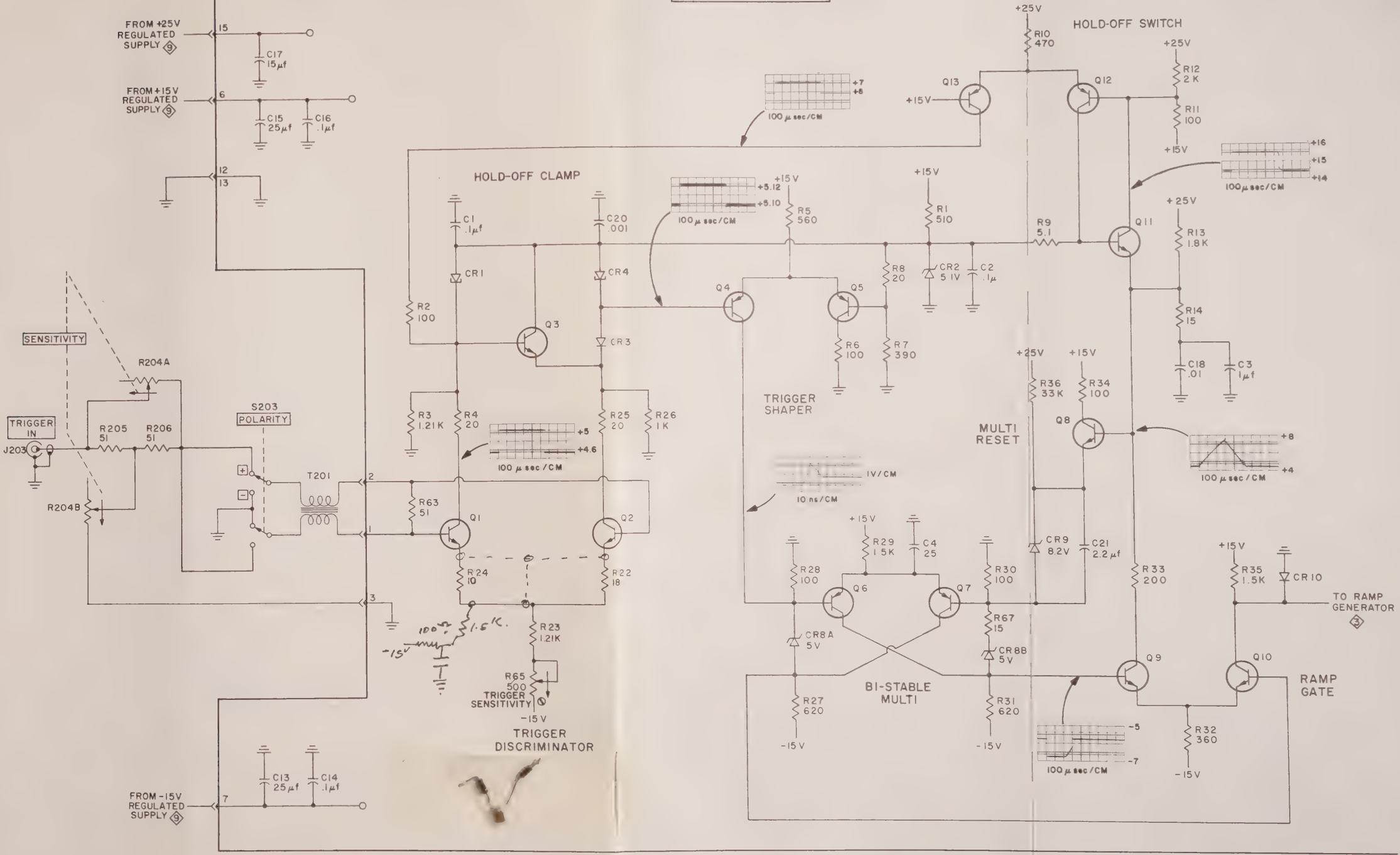


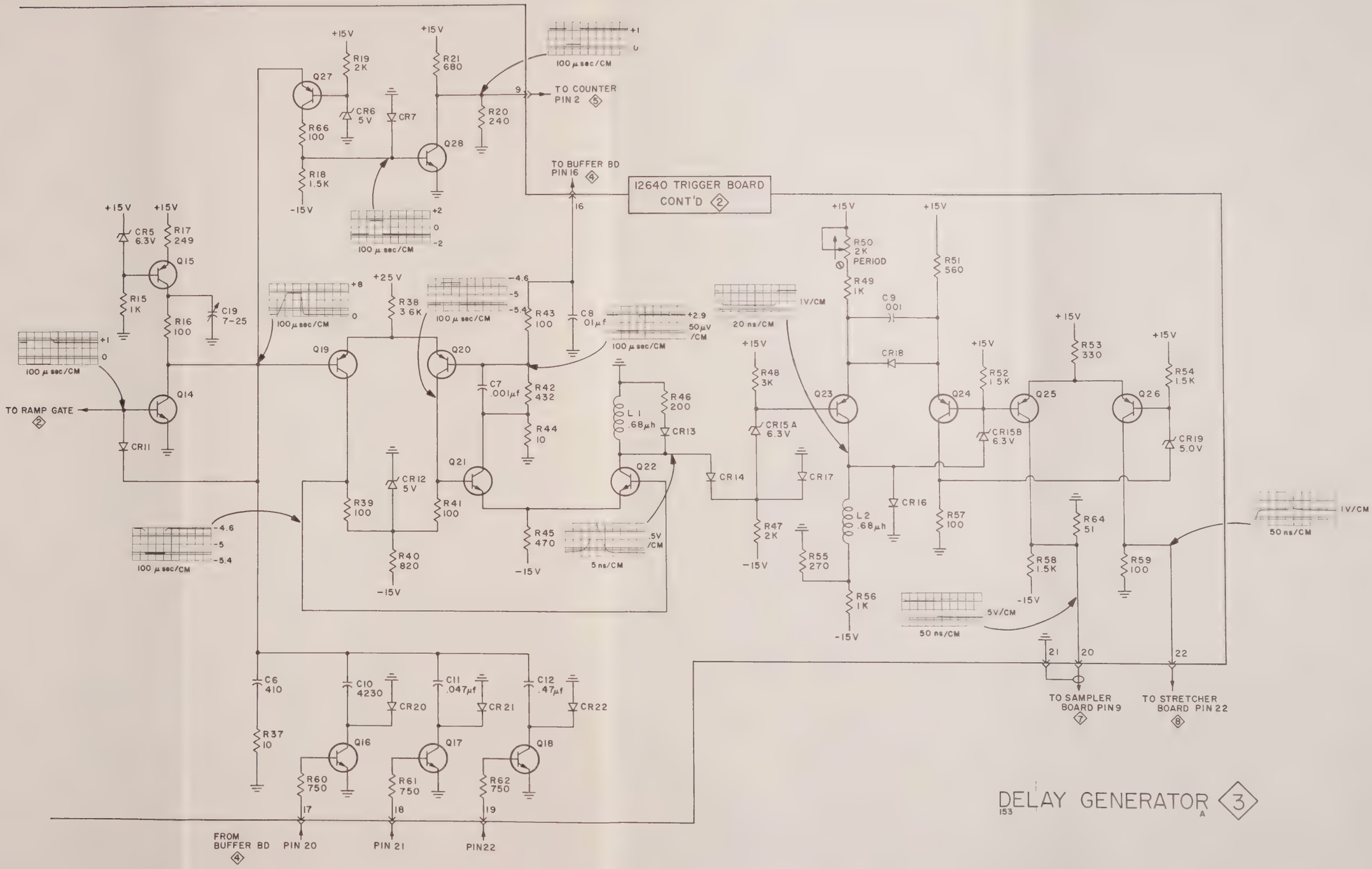
Fig. 6-9 Rectifier Board





153 BLOCK DIAGRAM (B)


FROM +25V REGULATED SUPPLY ⑨
FROM +15V REGULATED SUPPLY ⑨
C17 15μf
C15 25μf
C16 .1μf
HOLD-OFF SWITCH
+25V
R10 470
R12 2K
R11 100
+15V
Q13
Q12
100 μ sec/CM
HOLD-OFF CLAMP
C1 .1μf
C20 .001
CR1
CR4
CR3
R2 100
Q3
R3 1.21K
R4 20
R25 20
R26 1K
+5.12
+5.10
R5 560
R1 510
R8 20
CR2 5.1V
C2 .1μ
Q4
Q5
R6 100
R7 390
R9 5.1
Q11
R13 1.8K
R14 15
C18 .01
C3 1μf
+16
+15
+14
+5
+4.6
TRIGGER SHAPER
1V/CM
10 ns/CM
MULTI RESET
R36 33K
R34 100
Q8
+8
+4
SENSITIVITY
R204A
TRIGGER IN
J203
R205 51
R206 51
S203 POLARITY
T201
R204B
R63 51
Q1
Q2
R24 10
R22 18
100Ω
1.5K.
-15V
R23 1.21K
R65 500 TRIGGER SENSITIVITY
-15V
TRIGGER DISCRIMINATOR
FROM -15V REGULATED SUPPLY ⑨
C13 25μf
C14 .1μf
R29 1.5K
C4 25
R28 100
Q6
Q7
R30 100
CR9 8.2V
C21 2.2μf
R33 200
R35 1.5K
CR10
TO RAMP GENERATOR ③
CR8A 5V
CR8B 5V
R67 15
Q9
Q10
RAMP GATE
BI-STABLE MULTI
R27 620
R31 620
-15V
-5
-7
R32 360


12640 TRIGGER BOARD CONT'D 2
TO BUFFER BD PIN 16 4
TO COUNTER PIN 2 5
TO RAMP GATE 2
FROM BUFFER BD 4 PIN 20
PIN 21
PIN 22
TO SAMPLER BOARD PIN 9 7
TO STRETCHER BOARD PIN 22 8
+15V
-15V
+25V
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
CR5 6.3V
CR6 5V
CR7
CR11
CR12 5V
CR13
CR14
CR15A 6.3V
CR15B 6.3V
CR16
CR17
CR18
CR19 5.0V
CR20
CR21
CR22
R15 1K
R16 100
R17 249
R18 1.5K
R19 2K
R20 240
R21 680
R37 10
R38 3.6K
R39 100
R40 820
R41 100
R42 432
R43 100
R44 10
R45 470
R46 200
R47 2K
R48 3K
R49 1K
R50 2K PERIOD
R51 560
R52 1.5K
R53 330
R54 1.5K
R55 270
R56 1K
R57 100
R58 1.5K
R59 100
R60 750
R61 750
R62 750
R64 51
C6 410
C7 .001μf
C8 .01μf
C9 001
C10 4230
C11 .047μf
C12 .47μf
C19 7-25
L1 .68μh
L2 .68μh
100 μ sec/CM
5 ns/CM
20 ns/CM
50 ns/CM
1V/CM
5V/CM
50μV /CM
DELAY GENERATOR 3
153 A

12646 BUFFER BOARD

DELAY MULTIPLIER

R203 1K

R1 1.87K

R2 200 MULTI POT CAL

+15V

+25V

R3 12K

R4 49.9

S205 MULTI SOURCE

INT

EXT

DELAY ANALOG IN

J306

R207 1K

D/A

AUTO STEP

R5 1K

Q1

Q2

R9 1K

R8 12K

-25V

R6 536

R7 30K

-15V

TO D/A BOARD PIN 2 ⑥

DELAY ANALOG BUFFER

Q3

C1 .005μf

R14 3.9K

R10 2K

R11 2K

R12 249K

R13 20K ZERO

R15 1K

DELAY ANALOG OUT

J305

C

D

100nS

1μS

10μS

100μS

REMOTE

FROM J302 PIN 4

FROM J302 PIN 1

DELAY RANGE

S204

B

+36v

A

FROM J302 PIN 2

FROM J302 PIN 3

CR1 6.2V

R21 1.8K

R20 2K OFFSET

Q4

R19 1K

R18 100

R16 200 SCALE

R17 374

TO TRIGGER BD. PIN 16 ③

R24 4.3K

R22 390

R23 3.6K

Q5

Q6

R25 150K

R26 10K

100 μSec RANGE BUFFER

TO TRIGGER BOARD PIN 19 ③

R27 390

R28 3.6K

Q7

Q8

R29 4.3K

R30 150K

R31 10K

10μSec RANGE BUFFER

TO TRIGGER BOARD PIN 18 ③

R32 390

R33 3.6K

Q9

Q10

R34 4.3K

R35 150K

R36 10K

1μSec RANGE BUFFER

TO TRIGGER BOARD PIN 17 ③

FROM +25V REGULATED SUPPLY ⑨

FROM +15V REGULATED SUPPLY ⑨

FROM -15V REGULATED SUPPLY ⑨

FROM -25V REGULATED SUPPLY ⑨

12643 COUNTER BOARD

IC3A IC3B IC1D

IC14A IC8B IC8C IC8A IC7B IC7A IC14B IC9B IC9C IC15A IC9A IC9D IC15B

IC12A IC5C IC5A IC5B IC4B IC4A IC12B IC6B IC6C IC13A IC6A IC6D IC13B

IC10A IC1C IC1B IC1A IC10B IC2B IC2C IC11A IC2A IC2D IC11B

TO PIN 19

+3.6 V

R1 360 CR1 Q12 R2 1.5K C 3 800

R7 360 CR4 Q11 R8 1.5 K D 4 400

R3 360 CR2 Q10 R4 1.5K E 5 200

R5 360 CR3 Q9 R6 1.5K K 9 100

R9 360 CR5 Q8 R10 1.5K L 10 80

R11 360 CR6 Q7 R12 1.5K M 11 40

R13 360 CR7 Q6 R14 1.5K T 16 20

R15 360 CR8 Q5 R16 1.5K U 17 10

R17 360 CR9 Q4 R18 1.5K V 18 8

R19 360 CR10 Q3 R20 1.5K X 20 4

R21 360 CR11 Q2 R22 1.5K Y 21 2

R23 360 CR12 Q1 R24 1.5K Z 22 1

TO D/A BOARD 6

FROM +3.6 V SUPPLY 10

A 1 +3.6 V TO PIN 11 OF ALL IC'S

TO TRIGGER BOARD 3 PIN 9

2 'T' TO PINS 2 & 6 OF IC'S 10, 11, 12, 13, 14 & 15

12 13 TO PIN 4 OF ALL IC'S

TO J302 PIN 18 19

FROM COUNTER BOARD ⑤

1 2 4 8

12652 D/A BOARD 930-9

22 21 20 18

+15V SUPPLY ⑨

-15V SUPPLY ⑨

FROM COUNTER BOARD ⑤

10 20 40 80

17 16 11 10

TO S205 MULTI SWITCH AND BUFFER BOARD PIN 2 ④

FROM COUNTER BOARD ⑤

100 200 400 800

9 5 4 3

D/A CONVERTER 153 A ⑥

12634 SAMPLER BOARD

40ns DELAY LINE

SIGNAL IN J201

SIGNAL OUT J202

SHIELD

CRIA CRIB CRIC CRID

T2

R1 10K

C1 10

R2 5.1M

Q1 (A B)

R4 2K

Q2

CR2 5.0V

R3 10K

-15V$_F$

+15V$_F$

R9 1K

R8 1.1K

R10 4.22K

R11 10K

Q3 (A B)

R6 4.02K

R7 4.02K

R13 3K

Q4

Q5

R14 1.65K

R17 620

R18 47

R15 20

CR3 5.0V

C3 1.0µf

R12 200

-15V

TO STRETCHER BOARD PIN 16 (8)

TO STRETCHER BOARD PIN 17 (8)

R16 1K

C4 75

+15V

C9 0.1µf

R52 10

C11 1.0µf

C10 25µf

FROM +15V REGULATED SUPPLY (9)

12 13

R32 316

C7 1µf

R34 475

R35 1.82K

R36 200 GAIN

R33 470

CR4 5.0V

R31 2K

Q13

R29 4.99K

R30 100K

Q12

Q14

R28 100K

R27 10K

C6 1.0µf

R26 100

Q15 (B A)

R24 100

R25 71.5K

20

19

J302 OFFSET

R37 200K

R38 10K ZERO

R39 750K

21

ZERO R301 10K

C14 1.0µf

C13 25µf

C12 0.1µf

R53 10

7

FROM -15V REGULATED SUPPLY (9)

FROM TRIGGER BD PIN 20 (3)

9

8

R47 100

CLIP LINE

Q7 Q6

R51 470

R48 51

CR6 5.0V

R50 51

R49 330

R45 1.5K

CR5

Q8 Q9

R46 330

R44 51

R42 51

R43 300

Q11 Q10

R40 51

R41 51

R54 200

C8 .01µf

T1

C5 .002µf

R23 1K BALANCE

R22 15K

R21 1K

R20 1K

R19 15.4K

SAMPLER 7

153 (8)

12637 STRETCHER BOARD

TRIGGER AMPLIFIER

STROBE TIME TRIGGER AMPLIFIER

DATA RECORD TRIGGER GENERATOR

OUTPUT AMPLIFIER

MEMORY GATE GENERATOR

MEMORY GATE BRIDGE

SECOND MEMORY

FROM TRIGGER BD. PIN 22 ◇3

STROBE TIME TRIGGER OUT J304

DATA RECORD TRIGGER OUT J303

FROM SAMPLER BD. ◇7

PERIOD R51 10K

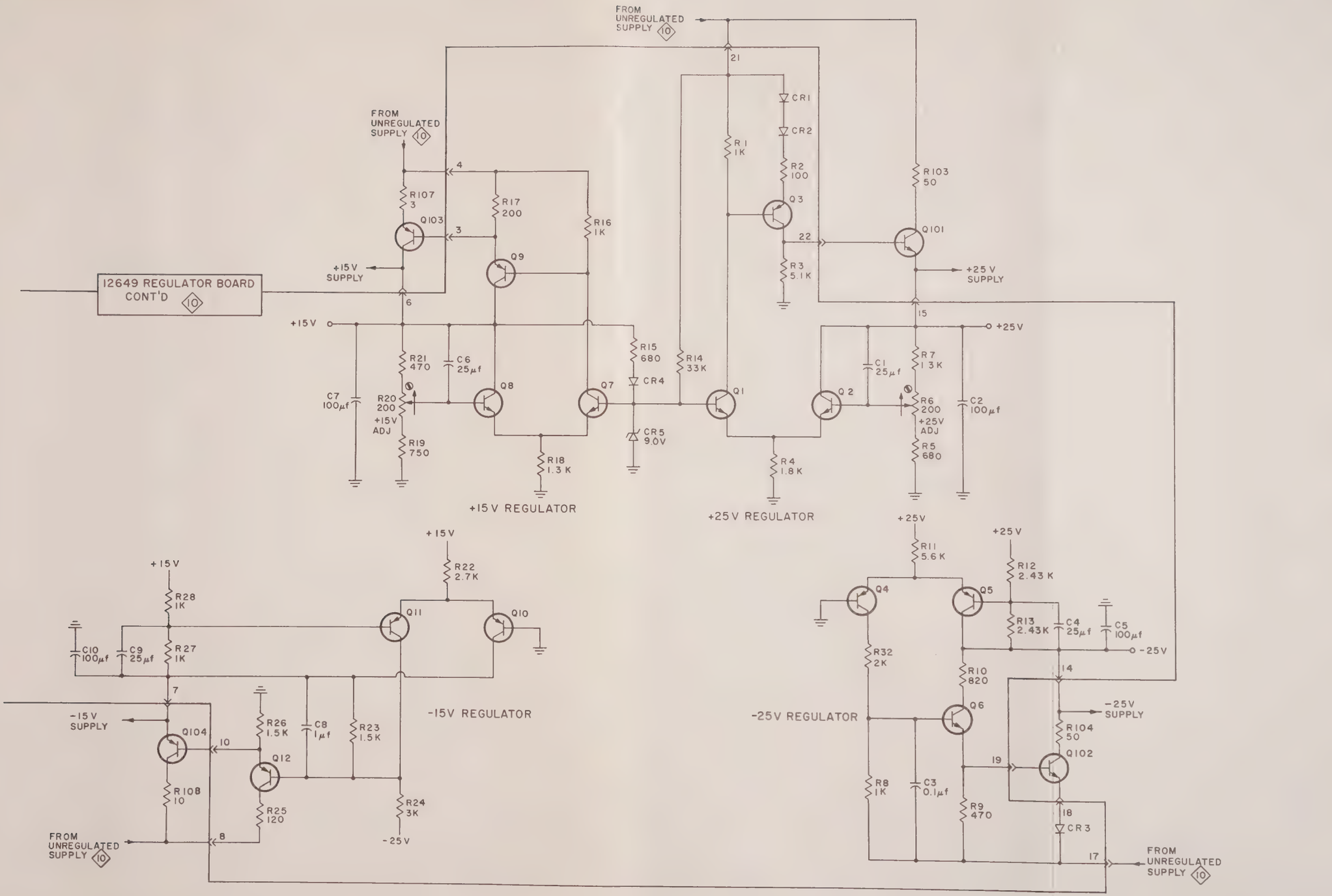
GAIN R20 200

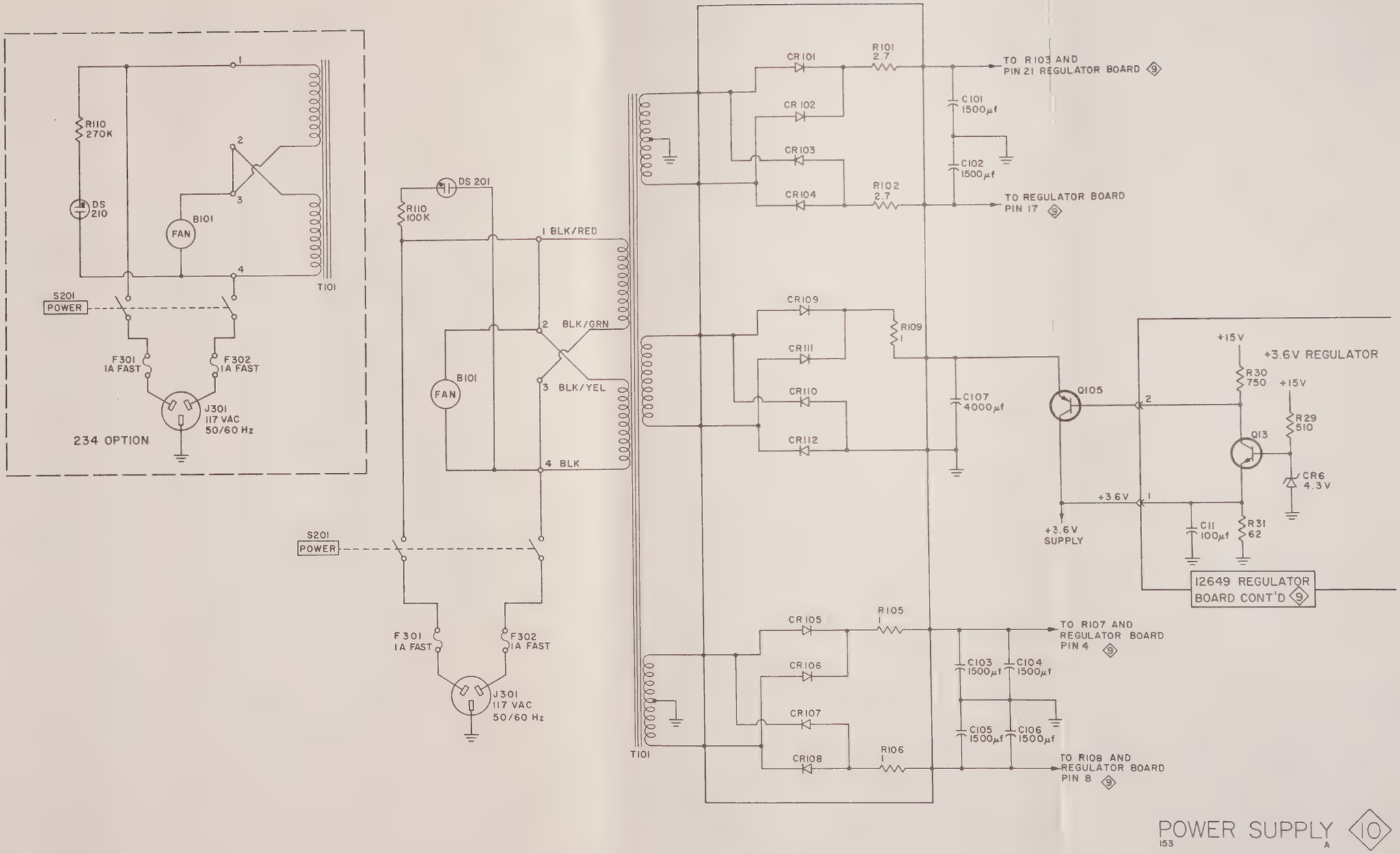
ZERO (1) R22 20K

ZERO (2) R37 20K

S202 GAIN X1 X10 X100

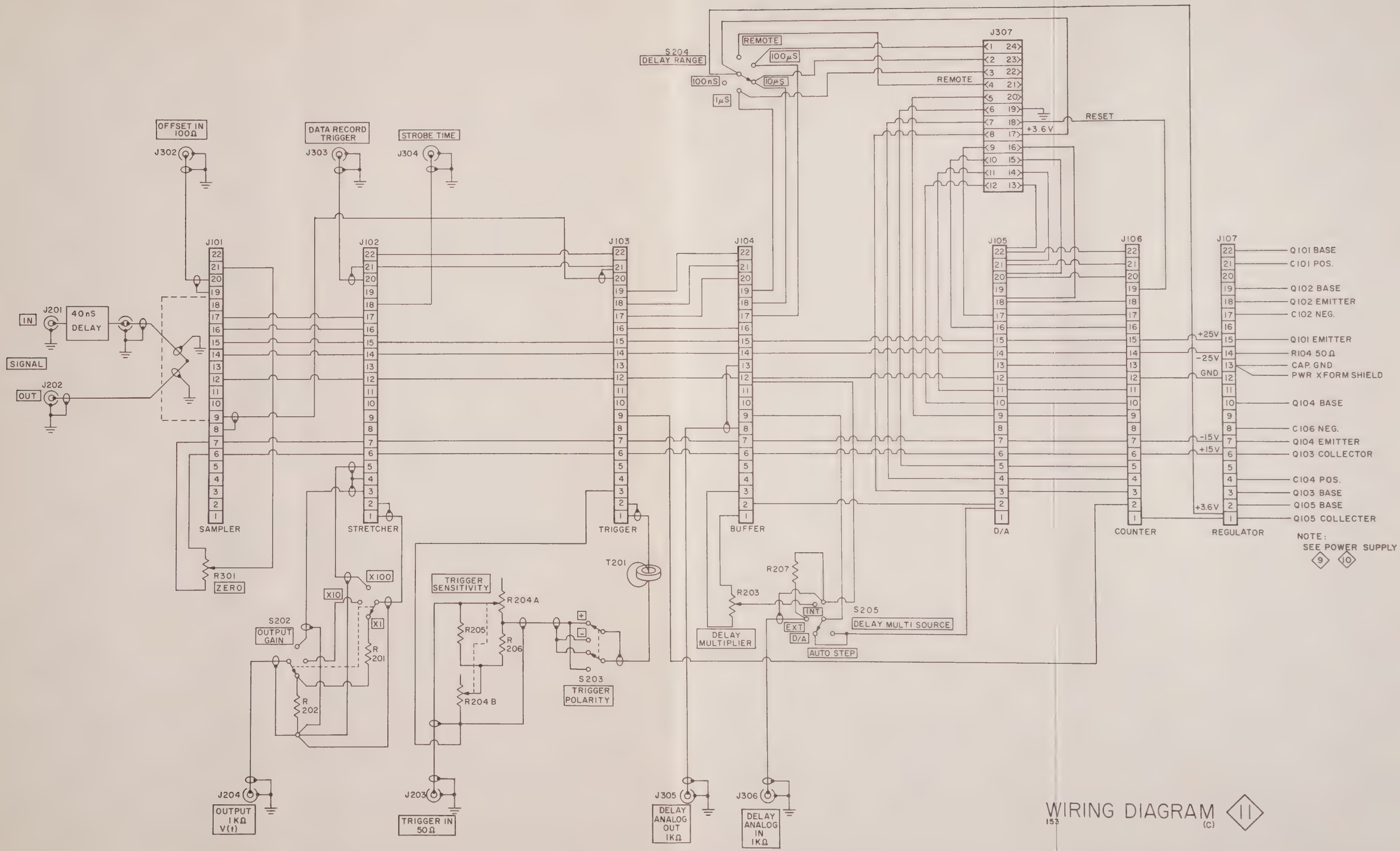
J204 1 KΩ V(t)


FROM UNREGULATED SUPPLY 10
12649 REGULATOR BOARD CONT'D 10
+15V SUPPLY
FROM UNREGULATED SUPPLY 10
21
CR1
CR2
R1 1K
R2 100
R103 50
Q3
Q101
22
R3 5.1K
+25 V SUPPLY
4
R107 3
Q103
3
R17 200
R16 1K
Q9
6
15
+15V
+25V
R21 470
C6 25μf
R15 680
R14 33K
C1 25μf
R7 1.3K
C7 100μf
R20 200 +15V ADJ
Q8
Q7
CR4
Q1
Q2
R6 200 +25V ADJ
C2 100μf
R19 750
CR5 9.0V
R18 1.3 K
R4 1.8K
R5 680
+15 V REGULATOR
+25 V REGULATOR
+15V
+25V
+15V
R22 2.7K
R28 1K
R11 5.6 K
R12 2.43 K
Q11
Q10
Q4
Q5
C10 100μf
C9 25μf
R27 1K
R13 2.43K
C4 25μf
C5 100μf
-25V
7
R32 2K
14
-15V SUPPLY
R26 1.5K
C8 1μf
R23 1.5K
R10 820
-25V SUPPLY
-25V REGULATOR
Q104
10
Q12
Q6
R104 50
R108 10
19
Q102
R8 1K
C3 0.1μf
R9 470
R25 120
R24 3K
18
CR3
FROM UNREGULATED SUPPLY 10
8
17
FROM UNREGULATED SUPPLY 10
-15V REGULATOR
-25V



POWER SUPPLY 10

153 A



WIRING DIAGRAM 11 (C)

153

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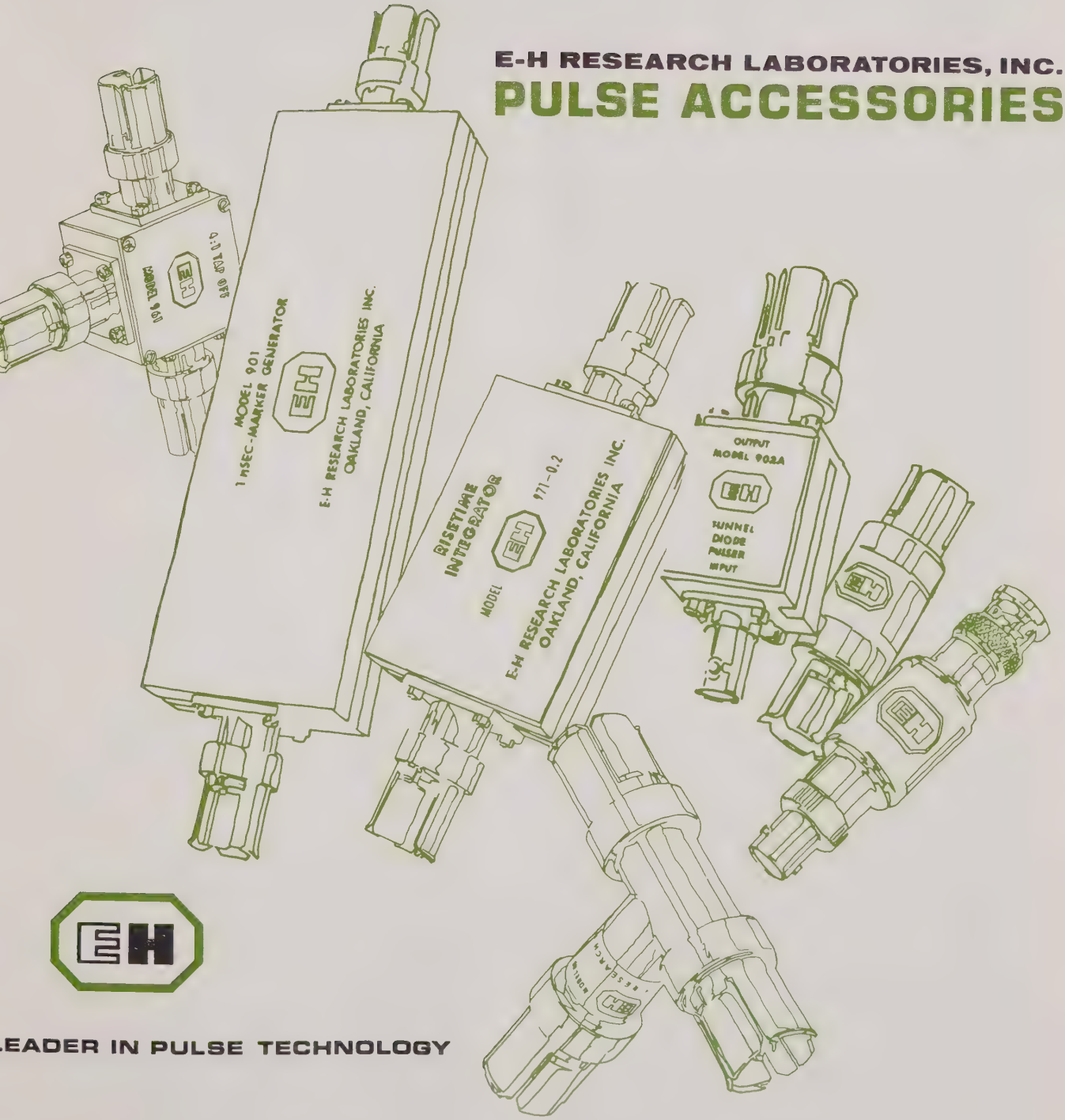
PULSE ACCESSORIES



EH

LEADER IN PULSE TECHNOLOGY

model 901 MARKER GENERATOR

The Model 901 Marker Generator is designed to convert a fast risetime voltage step into a train of time markers spaced precisely 1 nanosecond apart. The voltage output is proportional to the second time derivative of the leading edge of the input pulse.

SPECIFICATIONS

Marker Period . . . . . 1 nanosecond

Input Pulse Requirements . . . . . .approx. 100 ps risetime; pulse width greater than total markers to be used.

Marker Accuracy . . . . . .±0.3% non-cumulative from one marker to the next. Marker intervals are measured from either the peaks or the crossover point. Accuracy of ±0.1% is available on request.

Output Termination . . . . . .50 ohms

Input Termination . . . . . .50 ohms

Maximum Input Power . . . . . .0.1 watt minimum average

Attenuation Factor . . . . . .each marker's amplitude is approximately 1 dB down from previous marker.

Price $220

model 902A TUNNEL DIODE PULSER

The Model 902A contains a tunnel diode mounted in a high-frequency strip-line and supplies a 450 millivolt output with a risetime less than 100 picoseconds. This device may be driven with any period function such as a sine wave, square wave, ramp, etc. The Model 902A requires no power source other than its drive input.

SPECIFICATIONS

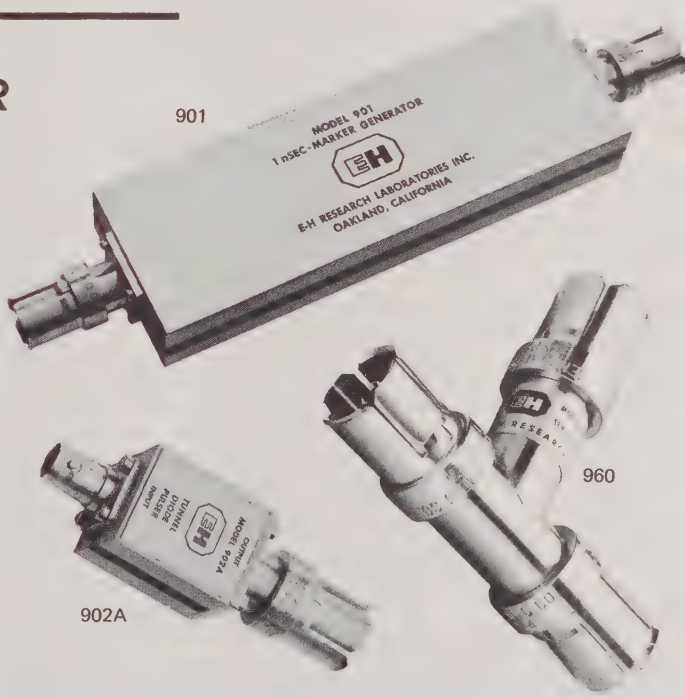
Polarity . . . . . .negative; positive on request

Pulse Distortion . . . . . .less than 10% (typically 5%)

Minimum Input Amplitude . . . . –5 volts peak into 50 ohms

Maximum Peak Voltage Input . . . . . 15 volts

Price $190



model 960 100:1 TAP-OFF

The Model 960 is a unique accessory in our product line: it is now possible to terminate a pulse system into 50 ohms and still observe the waveform without using the 50-ohm input impedance of the sampling oscilloscope as the load. This permits a 1 A pulser to be terminated with an adequate load, and still allows the pulse waveform to be observed without introducing distortion into the system.

The 960 has a risetime of 100 ps which is adequate for use with fast risetime pulsers such as the E-H Model 125A. With the advent of the 125A pulse generator and the 960 tap-off, an effective time domain reflectometry system may be set up with the use of the sampling scope.

SPECIFICATIONS

Risetime Input to Sidearm . . . . . less than 100 ps

Distortion Introduced Input to Output . . . . . less than 2%

Tap-Off Ratio . . . . . 100:1, ±3% into matched sidearm

Tap-Off Termination . . . . . oscilloscope connection must be terminated in 50 ohms for 100:1 ratio

Tap-Off Arm Distortion . . .less than 2% on 300 ps time scale
less than 6% on 100 ps time scale

Duty Cycle . . . . . .25% at 50 volts

Connectors . . . . . General Radio Type 874

Price . . . . . $ 90

model 961 *TDR TAP-OFF*

The 961 TDR Tap-Off is a 50-ohm line-sampling device designed to be used for time-domain reflectometry with the E-H Model 125A Pulse Generator. It delivers a 6 volt 300 ps step to the device under test with a 4:1 monitor tap-off ratio.

SPECIFICATIONS

Risetime Input to Sidearm ..... less than 300 ps

Distortion Introduced Input to Output ..... less than 2%

Input to Output Ratio ..... 1.66:1 ±5% (10–6)

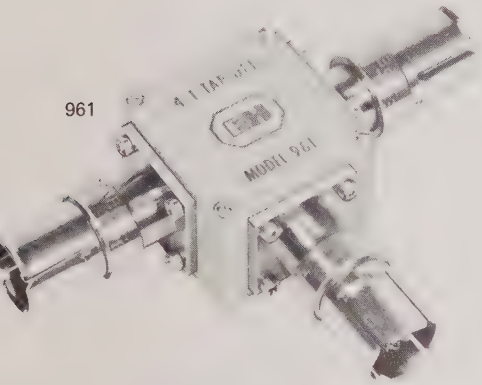
Tap-Off Ratio ..... 4:1 ±5% (output to arm)

Tap-Off Termination ..... 50 Ωscope input impedance forms the completion of arm

Tap-Off Arm Distortion ..... less than 2% on 300 ps time scale

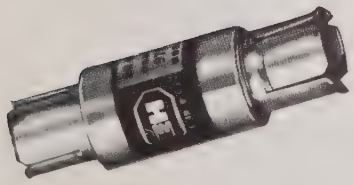
Duty Cycle ..... 10% at 10 V, maximum

Price $190



961

971



972

model 971 *RISETIME INTEGRATOR*

The Model 971 is a precision 50-ohm strip-line low-pass filter which is a useful pulse generator accessory for integrating fast-rising pulses to slower, precisely known, rise and fall times.

The Model 971 is made up of four half-section constant-k low-pass filters and is balanced so that either port may be used as an input. The specified risetime of the device is dependent on having an input much faster than its output risetime. A general rule would be to require the input to be ten times faster than the specified output. For inputs that do not meet this requirement, the resultant output risetime is equal to the square root of the sum of the squares of the input pulse risetime plus the risetime of the Model 971.

SPECIFICATIONS

Input Pulse Polarity ..... positive or negative

Risetime ..... 0.2 ns, 0.5 ns,1 ns, 2 ns and 5 ns

Accuracy ..... ±10% from 10% to 90% points with an input ten times faster than the specified output risetime.

Overshoot ..... less than 5%

Price $170

model 972 *PULSE TRANSFORMER*

The Model 972 is a 50-ohm to 50-ohm inverting transformer which has an extremely fast risetime. The 972 was designed primarily to invert the 120E pulse generator output but will find many other useful applications in pulse work, such as dc isolation, and matching which requires 1:1 impedance ratios.

SPECIFICATIONS

Risetime ..... less than 0.25 ns

Distortion ..... 5% on a 300 ps time base

Pulse Width ..... maximum 1 μs at 10 V with 37% droop.

Price ..... $ 90

model DT DC RESTORER

This diode device eliminates baseline shift in ac-coupled, nanosecond-pulse systems. The Model DT clamps to 0 volts.

SPECIFICATIONS

Peak Input	20 V
Attenuation	approximately 10%
Uses	DTP for positive pulses, DTN for negative pulses.
Price	$ 60

model RT RISETIME INTEGRATOR

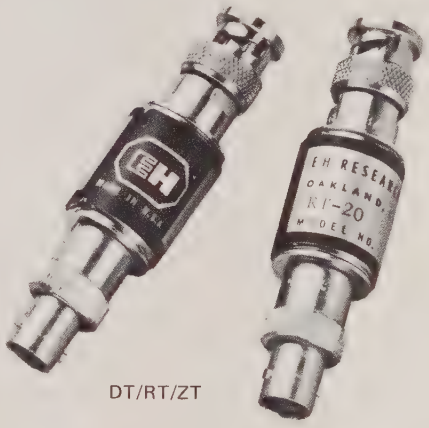
This device is used to produce known, repeatable, fixed times from a fast pulse input.

SPECIFICATIONS

Standard Times	5, 10, 20, 50, 100 ns (special times available on request)
Accuracy	±10%
Maximum Average Input	500 mA
Connectors	BNC

Specify risetime when ordering (e.g., RT-10 = 10 ns).

Price ..... $ 35



DT/RT/ZT

model ZT PULSE TRANSFORMER

This nanosecond transformer is used for impedance matching or inversion. Impedances of 50, 93, 125, 185, or 200 ohms are available. Any combination input to output with or without inversion can be accomplished. BNC connectors are provided.

ORDERING INFORMATION FOR THE MODEL ZT

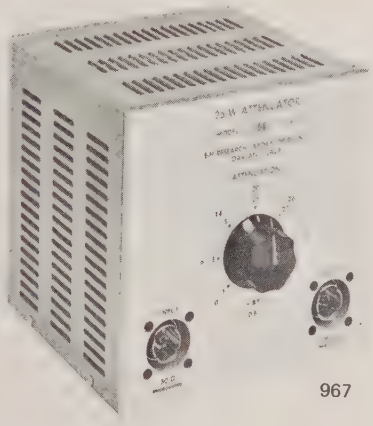
Input Impedance: specify first digit if below 100 ohms or first two digits if 100 ohms or above.

Output Impedance: same as above.

Inversion: if inversion is required add an X at the end of the model number.

Example: Model ZT-5-20X: 50 ohms input impedance; 200 ohms output impedance; inverted output.

Price ..... $ 35



967

model 967 ATTENUATOR

The E-H Model 967 Variable Attenuator is a 50-ohm high power switching attenuator for fast-pulse systems.

Features of the 967 include:

1. Less than 2% pk–pk clutter at 5 ns
2. 1/2/5/10/20/50/100:1 steps
3. 25 watt average dissipation

Price $290

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TP5M/PA1272

Prices and technical data subject to change without notice – All prices F.O.B. Oakland, California

CHANGE INFORMATION

The following types of changes are found in this Section:

Corrections--
changes due to errors in text or illustrations

Additions--
new text or new illustrations to supplement original manual

Revisions--
new text or new illustrations to up-date original manual

Options--
information on non-standard accessories or options available for this instrument

Modifications--
information on special features of a custom-designed instrument

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